Deutsches Zentrum
DLR für Luft- und Raumfahrt

Design and Feasibility Study of a High-Speed SerDes Communication Backbone for a Zonal Robotic Hand Architecture

Master Thesis

Modern robotic hands integrate dense sensor/actuator networks in zones, but their complex, multi-protocol wiring creates challenges in weight and latency. This thesis investigates replacing this with a unified, high-speed serial (SerDes) backbone. Inspired by automotive zonal architectures, this all-hardware protocol aggregates diverse data (video, sensor, control) onto one link, promising the ultra-low, deterministic latency vital for robotic control.

After analyzing the robotic hand's data-flow requirements, the student will design and build a functional hardware prototype of this zonal backbone. This involves integrating all-hardware protocol IP cores onto FPGA evaluation boards. The final goal is to evaluate this architecture and present a final demonstration showing the aggregation and transmission of camera and sensor data over the unified link, proving its feasibility.

Prerequisites:

- Excellent practical experience with FPGAs, specifically with Xilinx (Vivado) or Lattice (Radiant/Diamond) development toolchains. This is essential.
- Strong familiarity and project experience with VHDL for IP core integration and logic design.
- Solid hands-on skills in digital electronics and prototyping: experience interfacing evaluation boards, managing signal integrity, and debugging hardware.
- Good understanding of communication protocols (e.g., SPI, I2C, and ideally MIPI CSI-2 for cameras).
- [Advantageous] Practical experience with embedded C for soft-core processors (e.g., MicroBlaze) for control or test-bench setup.

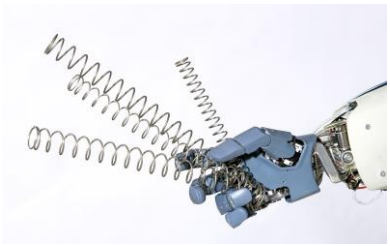

Fig. 1: SerDes-based Communication for a Robotic Hand

Tasks:

- Literature research on high-speed, low-latency SerDes communication, all-hardware protocols, and zonal architectures in robotics.
- Analysis and quantification of the data-flow requirements (bandwidth, latency, synchronisation) for the robotic hand's components (cameras, sensors, actuators).
- IP Core Integration: Integrate the provided all-hardware protocol IP core(s) onto the FPGAs. Establish a stable, high-speed communication link between two (or more) "zonal" nodes.
- Interface Development: Design and implement the "gateway" logic in VHDL that bridges data from sensors (via SPI/I2C) and cameras (via MIPI) to the hardware aggregation IP core.
- Prototype Validation: Conceive and execute tests to measure the real-world performance of the hardware prototype, focusing on end-to-end latency and data throughput.
- Final Demonstration: Assemble a hardware demonstrator that visibly shows the principal communication interface in action (e.g., streaming camera video and sensor data from one node to another over the unified link).

Start: At the earliest possible date
Contact: oliver.neumann@dlr.de

Please include a brief motivation, a CV, a copy of your transcripts in your application. This work will be conducted in Oberpfaffenhofen with visits to the industry partner.

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