High Throughput FEC Requirement

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Version: V1.0(20190228)

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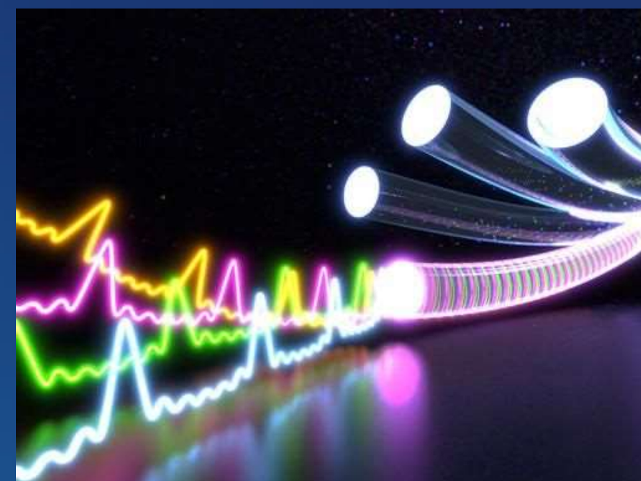
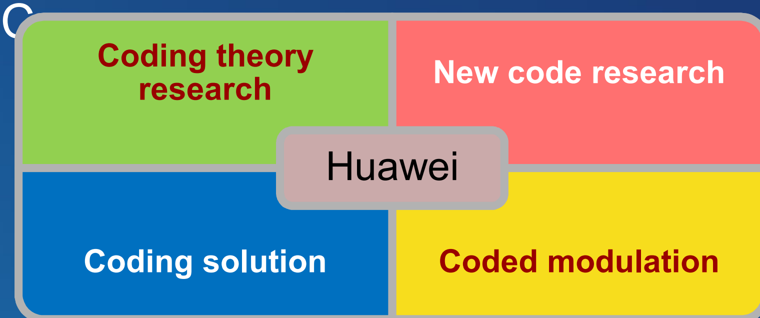
Outline

- **Background**
  - Optical communication boost
  - Challenge and solution
- **High throughput coding issues**
  - Key questions for high throughput FEC
  - System Optimization
- **Summary**





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Optical enabled Instrumentation, Connection and Intelligence

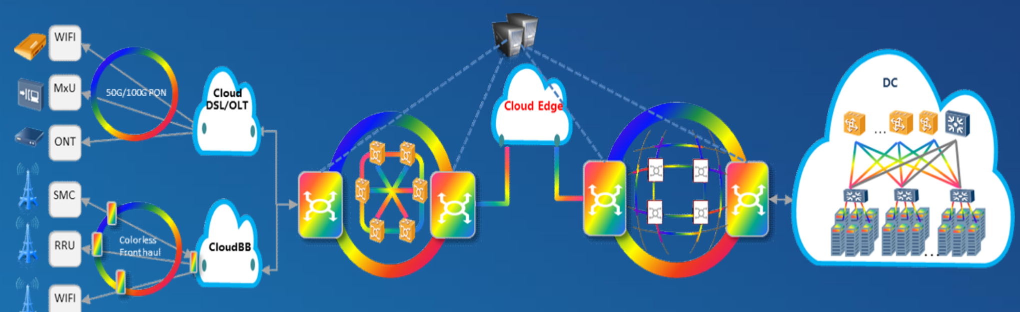
- **Communication** is the most important direction of Optical technologies
- Huawei already entered new market of optical technologies: like Vehicle, Sensor, computing etc.

Sensing ← **Connecting** → **Computing**

Optical Sensor

- Laser Radar
- Fiber Sensing
- MEMS Sensing
- Novel Display
- Bio-optical Sensing
- THz Optics

Optical Communication



Building a cloud-oriented, all-space-integrated all-optical network

- Novel Fiber Communication
- Space Optical Communication
- Quantum Communication
- THz Communication

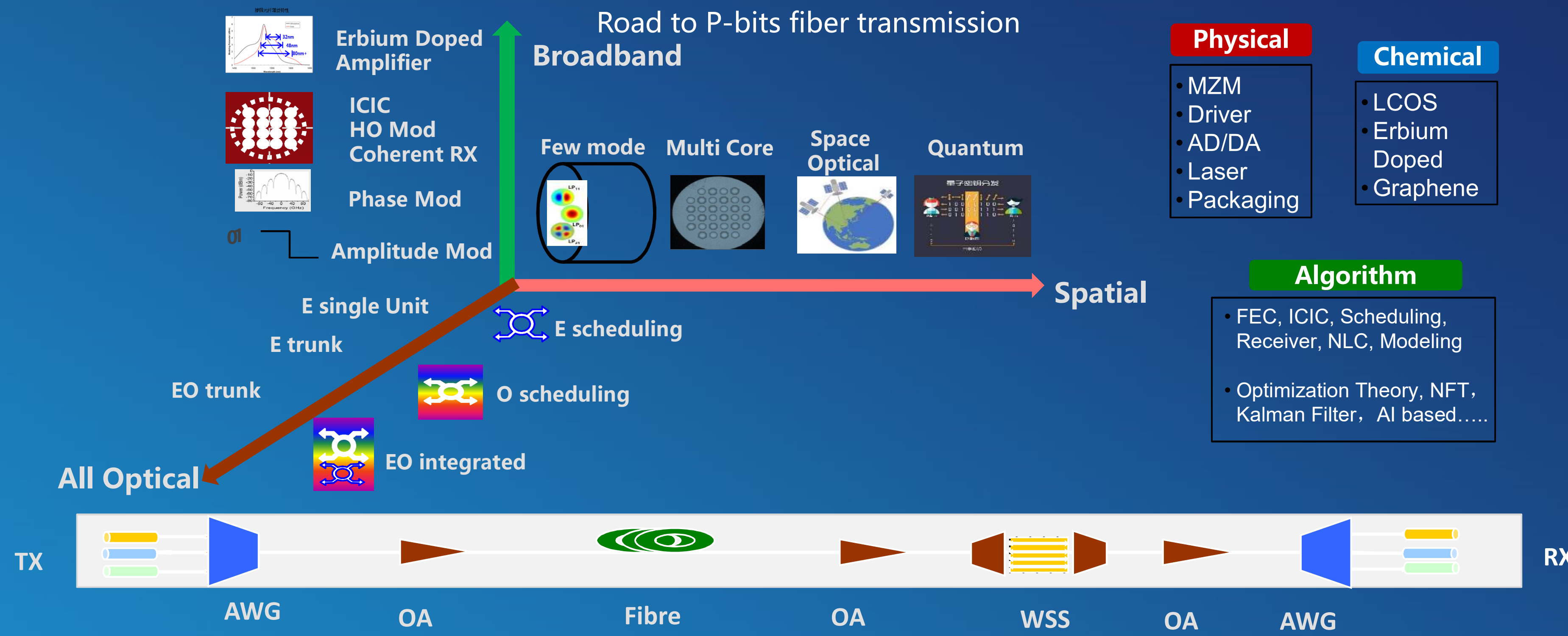
Optical Computation

- Quantum computing
- Optical Computing
- Optical Neural Network
- Optical Memory

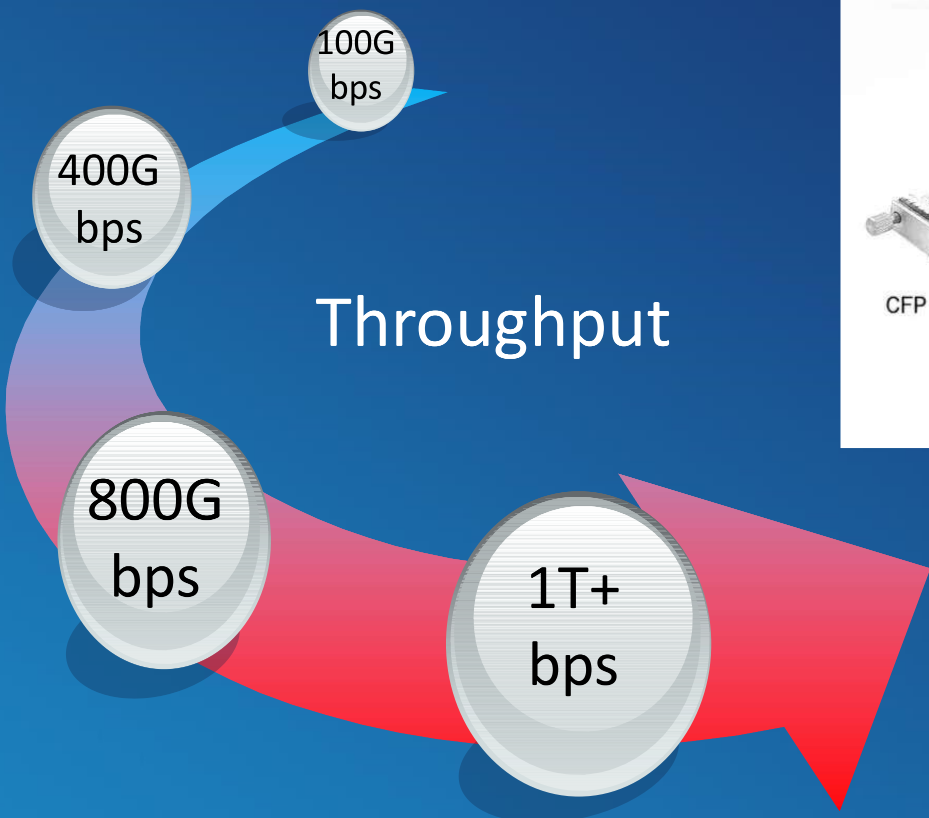
- Optical Network Architecture
- Optical Crossing
- Photoelectric Integration
- Optical Module
- Optical Algorithm
- Optical Control
- Space Optics
- Spectroscopy

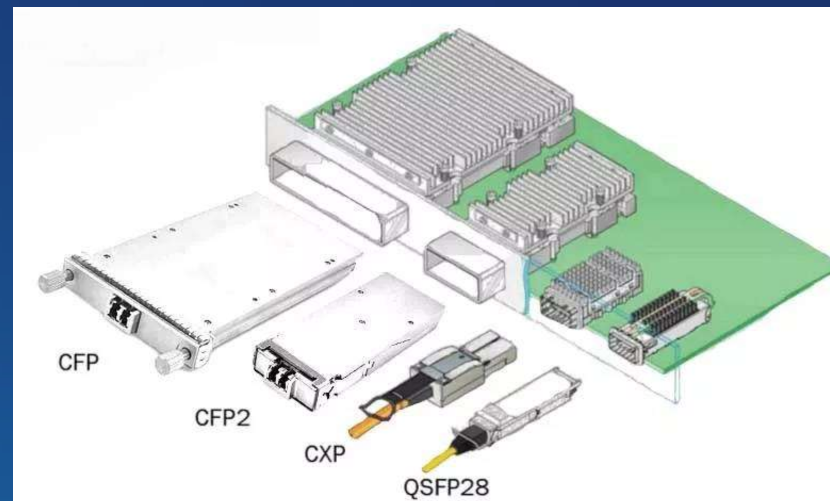
100x BW boost

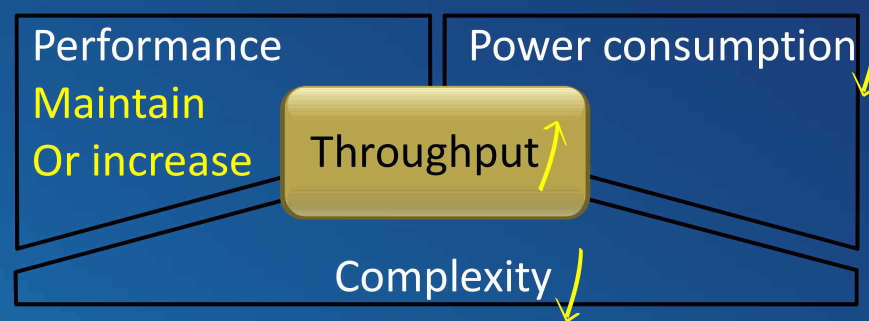
- Nonlinear compensation and **FEC** can improve the limit performance with the cost: complexity
- New Receiver, **FEC** and **cross boundary design** may help us to achieve 100x BW increase



Optical Transmission Trends



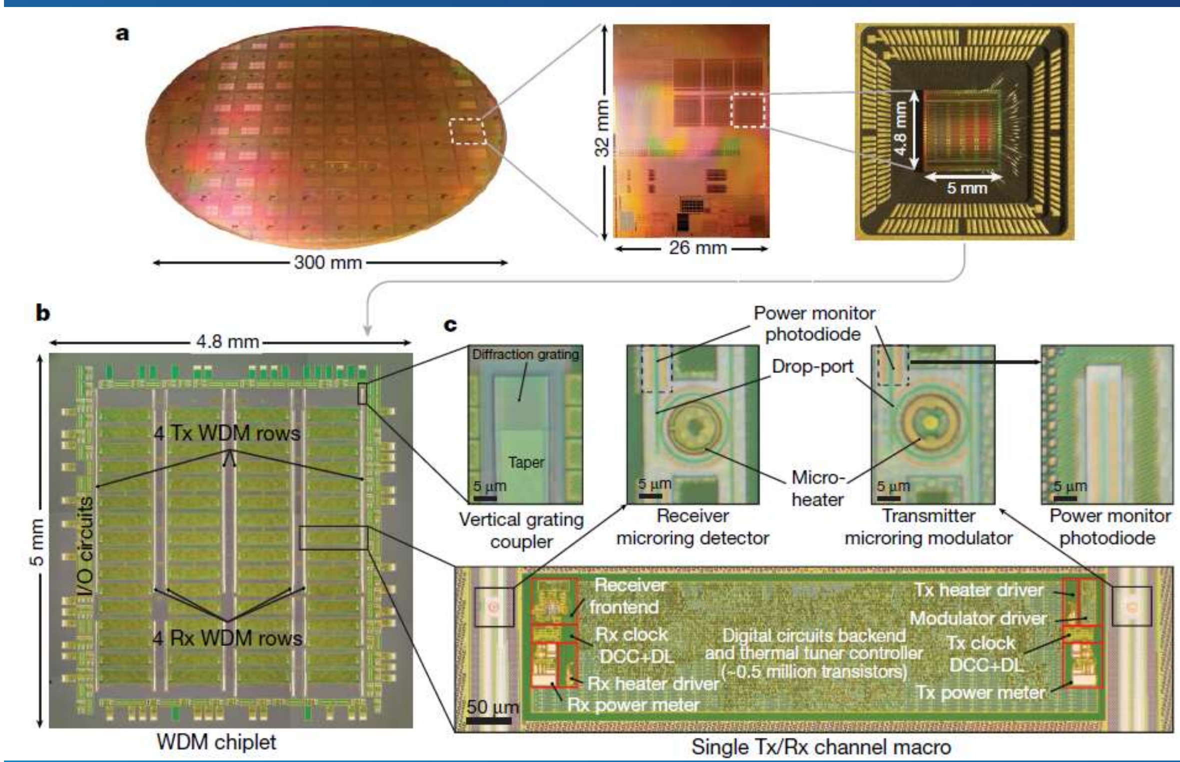




- **Maintain or decrease power consumption & complexity when throughput increase?**

How to reach Future?

Monolithic electronic-photonic platform



Atabaki, Amir H., et al. "Integrating photonics with silicon nanoelectronics for the next generation of systems on a chip." *Nature* 556.7701 (2018): 349.

Fabrication improvement

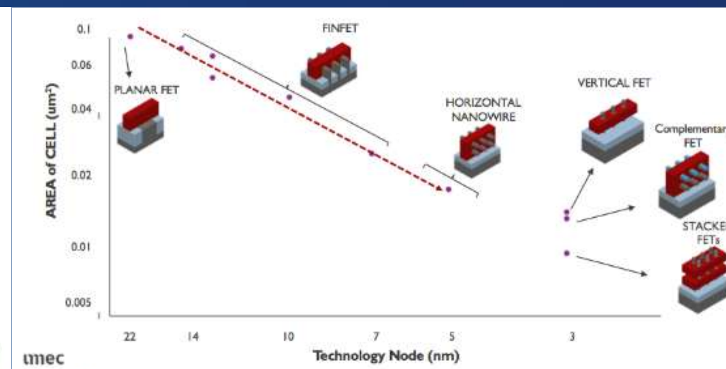
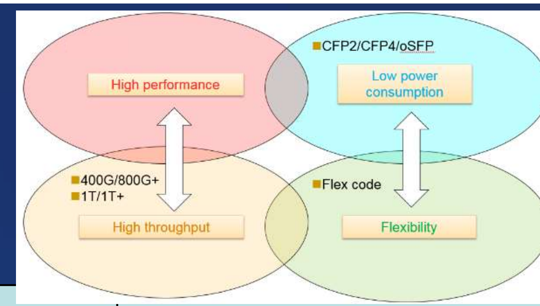


Fig. 1: Next-gen transistor architectures. Source: Imec/ISS

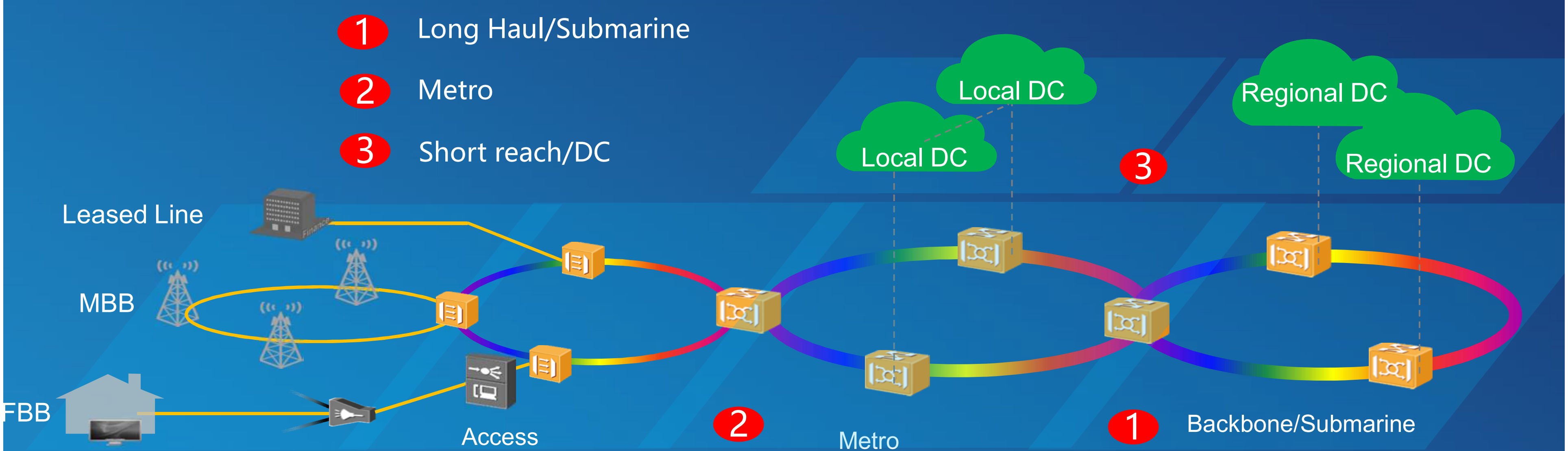
Analog part benefit less and wires cost a lot.

Algorithm reduce complexity and power cost!

High throughput FEC?



Scenario	FEC Requirement	Modulation (+CS)	FEC type
Long Haul/Submarine	High Performance, error floor<1E-15 Large OH, Soft decoder,	BPSK/QPSK/16QAM/64QAM...	LDPC(C)/TPC(C)/...?
Metro/DCI	Performance V.S. Power, error floor<1E-15 Large OH, Soft decoder, anti-burst	QPSK/16QAM/64QAM/128QAM/...	LDPC(C)/TPC(C)/...?
Short reach/DCN	Low Latency & Power Cost, error floor<1E-15 Small OH, Hard decoder, anti-burst	PAMx/NRZ/...	KP4/RS/Staircase/TPC...?



Short Reach/DCN high throughput

Short reach/DCN	Low Latency & Power Cost, error floor<1E-15 Small OH, Hard decoder, anti-burst	PAMx/NRZ/…	KP4/RS/staircase/TPC…?

OH, %		Length, bits	InBER@1e-15, AWGN	Latency (Encoding + Decoding)	Interleaver Latency	Total Latency
6	BCH	8K	9.2e-4	≈ 160 ns	≈ 110 ns	≈ 270 ns
6	RS(KP4)	5K	2.2e-4	≈ 80 ns	–	≈ 80 ns

- **Ultra-high speed (throughput), 400G~800G~1T+ bps**
- **Device or IP Bandwidth limited 25G+**
- **V.S. KP4, 10x performance, similar latency?**
- **Standardized FEC, compatible**
- **Hard or soft**
- **Burst Channel**
- **Error floor <1E-15**

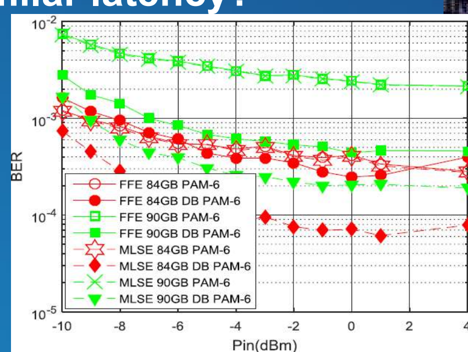
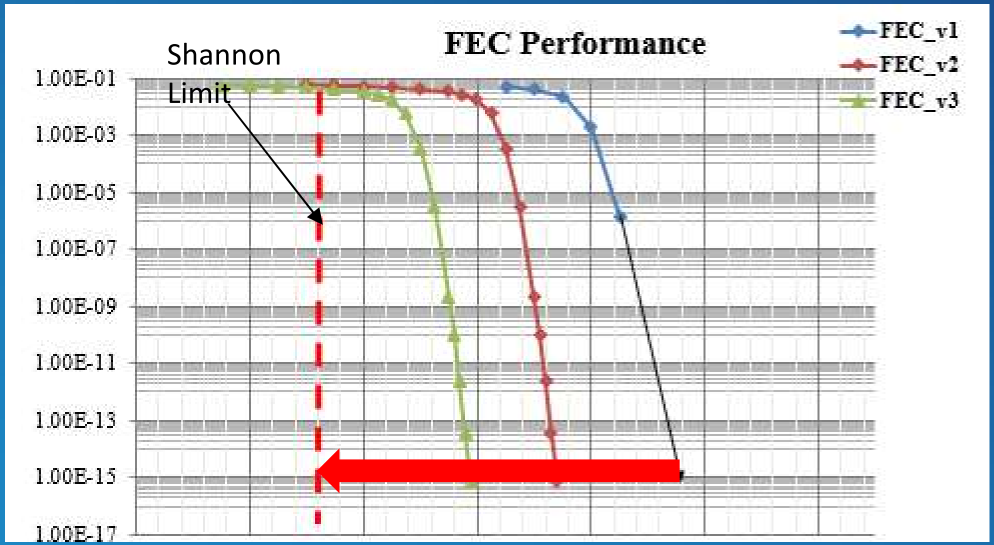


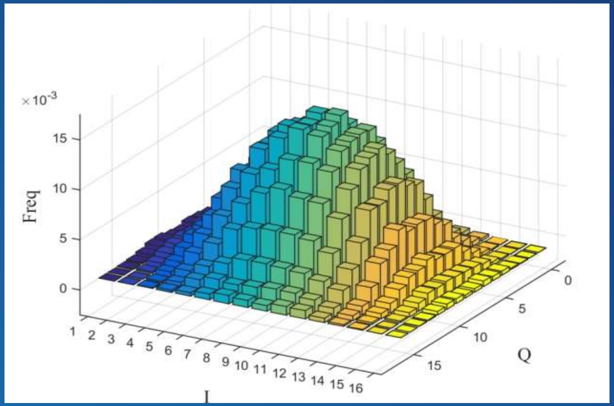
Fig. 4: BER performance of PAM-6 and DB PAM-6

High performance & low power consumption

Long Haul/Submarine	High Performance, error floor<1E-15 Large OH, Soft decoder,	BPSK/QPSK/16QAM/64QAM…	LDPC(C)/TPC(C)/…?

- **Ultra-high speed (throughput), 400G~800G~1T+bps….**
- **Ultra-high performance, approaching Shannon limit**
- **Low power consumption & complexity decoding algorithm**
- **Joint FEC and Shaping design for 16 or 64QAM+**





LDPC solution

LDPC Solution

LDPC Type

- Binary
- Non-binary
- Regular/Irregular
- Spatially coupled
- Generalized
- …

Decoding algorithm

- BP
- Generalized BP
- Min-sum
- Offset Min-sum
- Scaled Min-sum
- Adjust Min-sum
- …

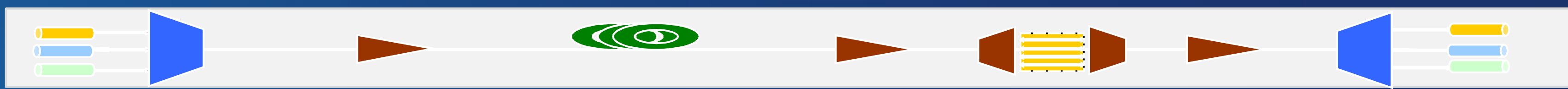
Which combination is the best choice, considering the criteria?

Key Criteria

Performance/Complexity/Power Consumption/throughput

Complexity ≠ Power Consumption (active complexity + static power consumption)

FEC for different modulation



Fixed optical module IP core, modulation influence the performance much. Quality of LLR would influence decoder! FEC + Modulation design based on system quality!

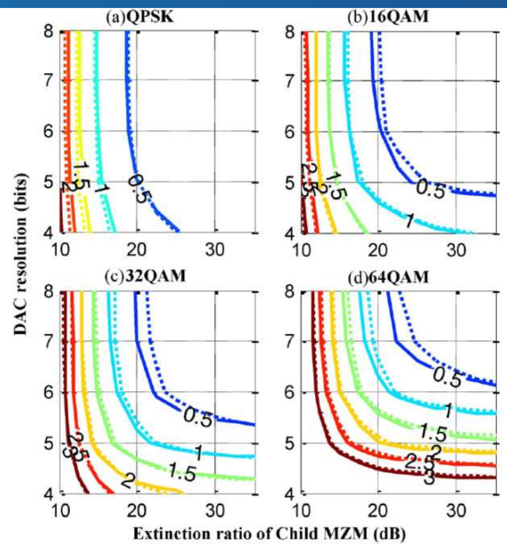


Fig. 3. Contour plots of Q-factor penalty versus the resolution of the DAC and the ER of the child MZM with (solid line) predistortion and without (dashed line) predistortion for (a) 4-QAM, (b) 16-QAM, (c) 32-QAM, and (d) 64-QAM.

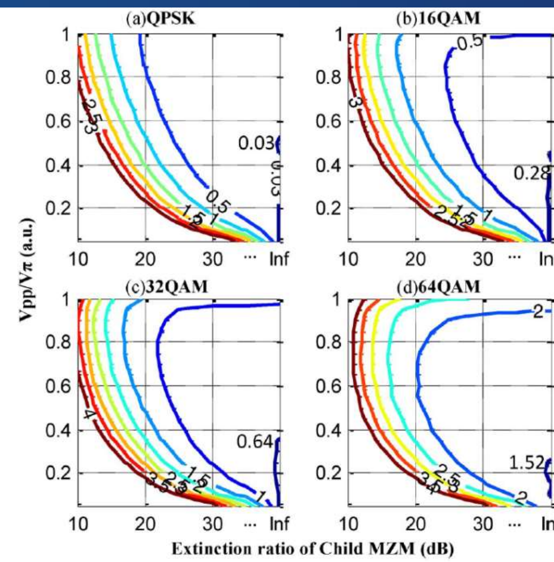


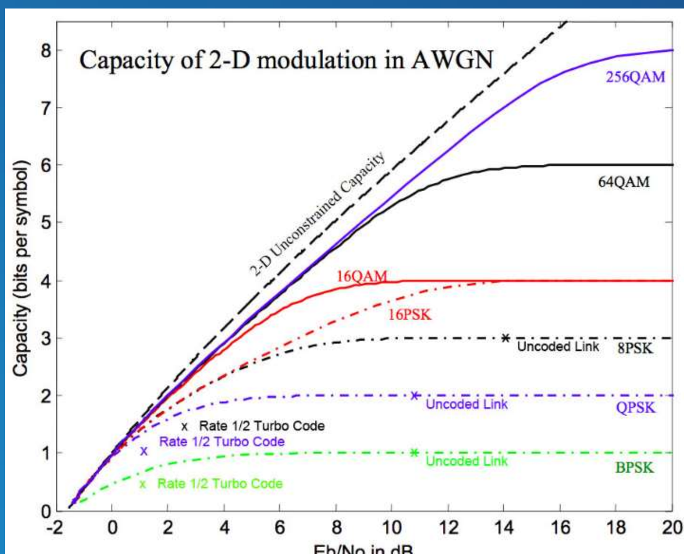
Fig. 4. Contour plots of Q-factor penalty against the Vpp of the driving signal and the ER of the child MZM for (a) 4-QAM, (b) 16-QAM, (c) 32-QAM, and (d) 64-QAM.

Huang L, Guo C, He S. Design and analysis of a CO-OFDM transmitter with limited modulator extinction ratio[J]. IEEE Photonics Journal, 2014, 6(3): 1-7.

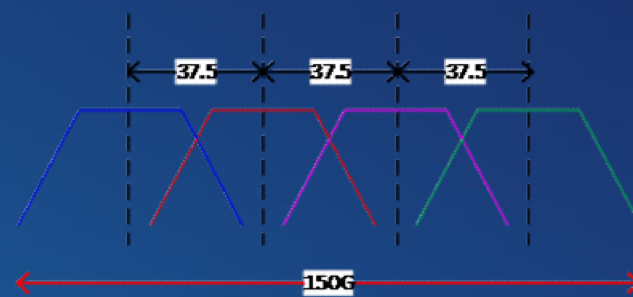
Information and coding theory for channel with interference and memory

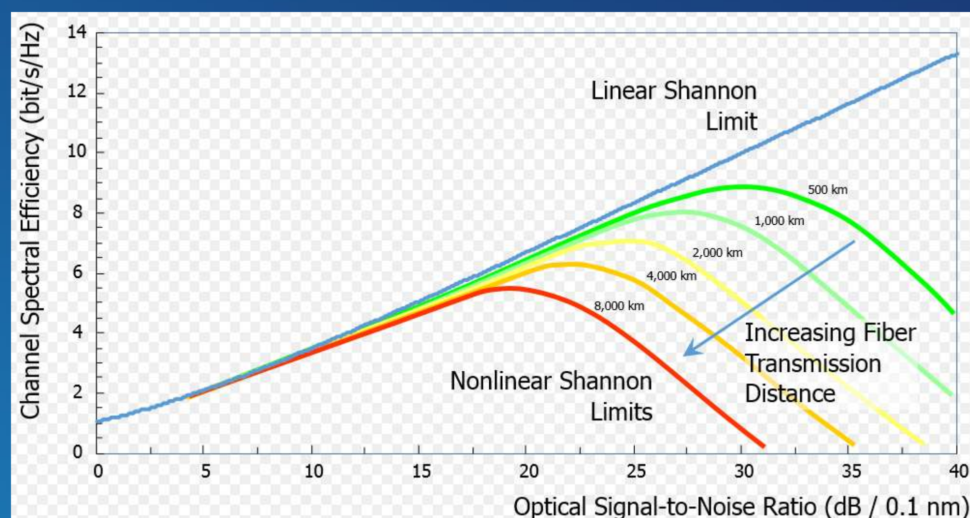
Shannon limit(1948)—AWGN channel

$$C = B\log_2\left(1 + \frac{S}{N}\right)$$



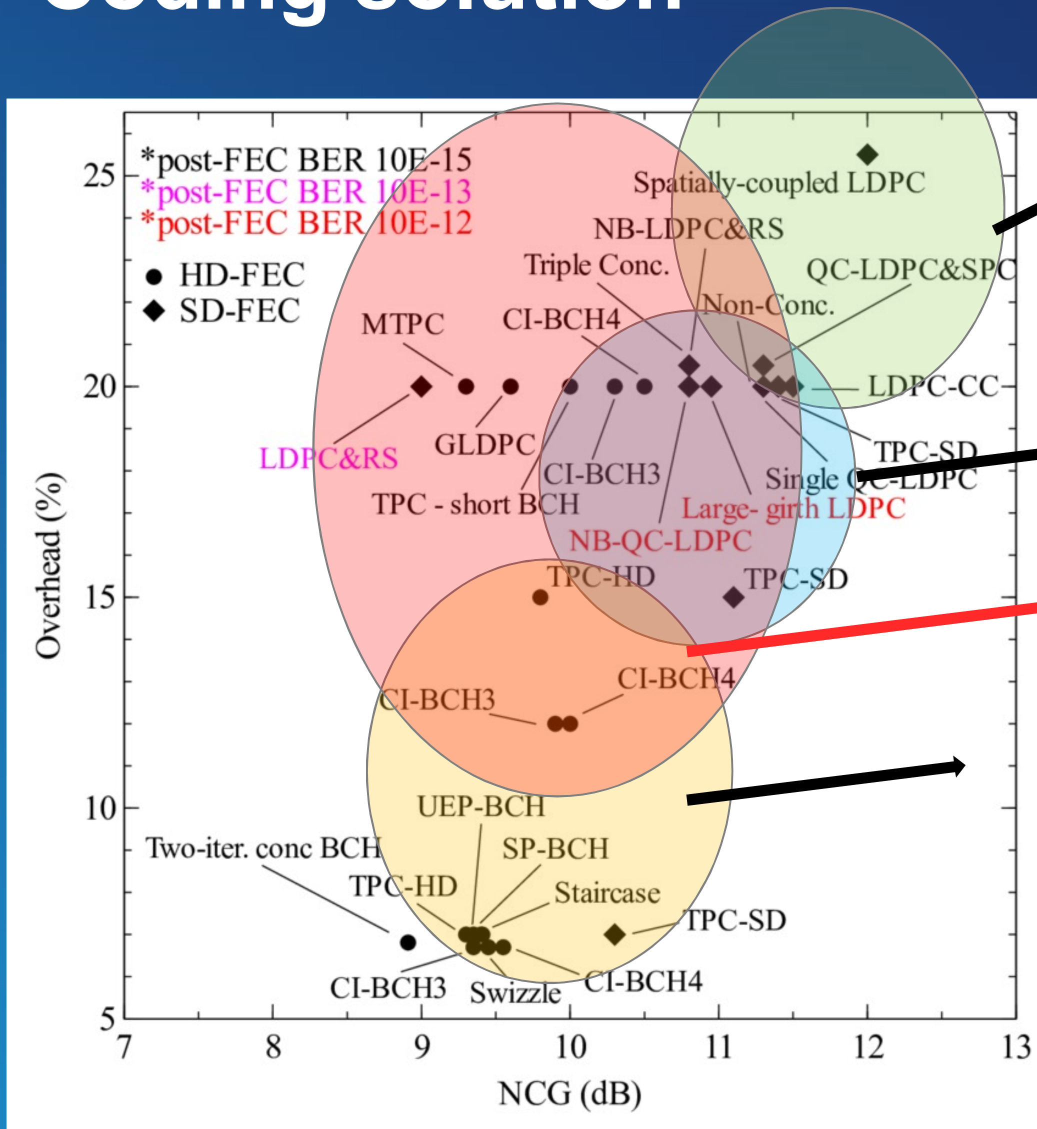
XX Limit—Interference and Memory channel





Theory of Coding, Modulation and Shaping for channel with interference and memory?

Coding solution



High performance: Long Haul/Submarine

Low power consumption: Metro/DCI

FEC for Metro & Long Haul
FEC for Metro & DC

Low power consumption & Low latency: Short reach/DCN

Summary

- **FEC Optimization for High Throughput**
  - Low power consumption decoder design
  - Joint FEC, Modulation, and Shaping
  - Nonlinear or interference condition optimization
  - Specific design for different modulation for fixed channel
  - …
- **Revolution of system?**
  - FEC (coded modulation) for MIMO (few mode or multi-mode or OAM transmission)?
  - Tbps+ Challenge, CMOS benefit reduce as IP cost much

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BUILDING A BETTER CONNECTED WORLD

THANK YOU

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