Information Optimized Quantized Message Passing for Near-Tbps Fully Pipelined LDPC Decoding

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Telecommunications Circuits Laboratory

Low Density Parity Check (LDPC) Codes

1962: invented by **R. G. Gallager**

- Performance close to the Shannon limit
- Iterative decoding was initially **considered to complex for** economic **implementation**

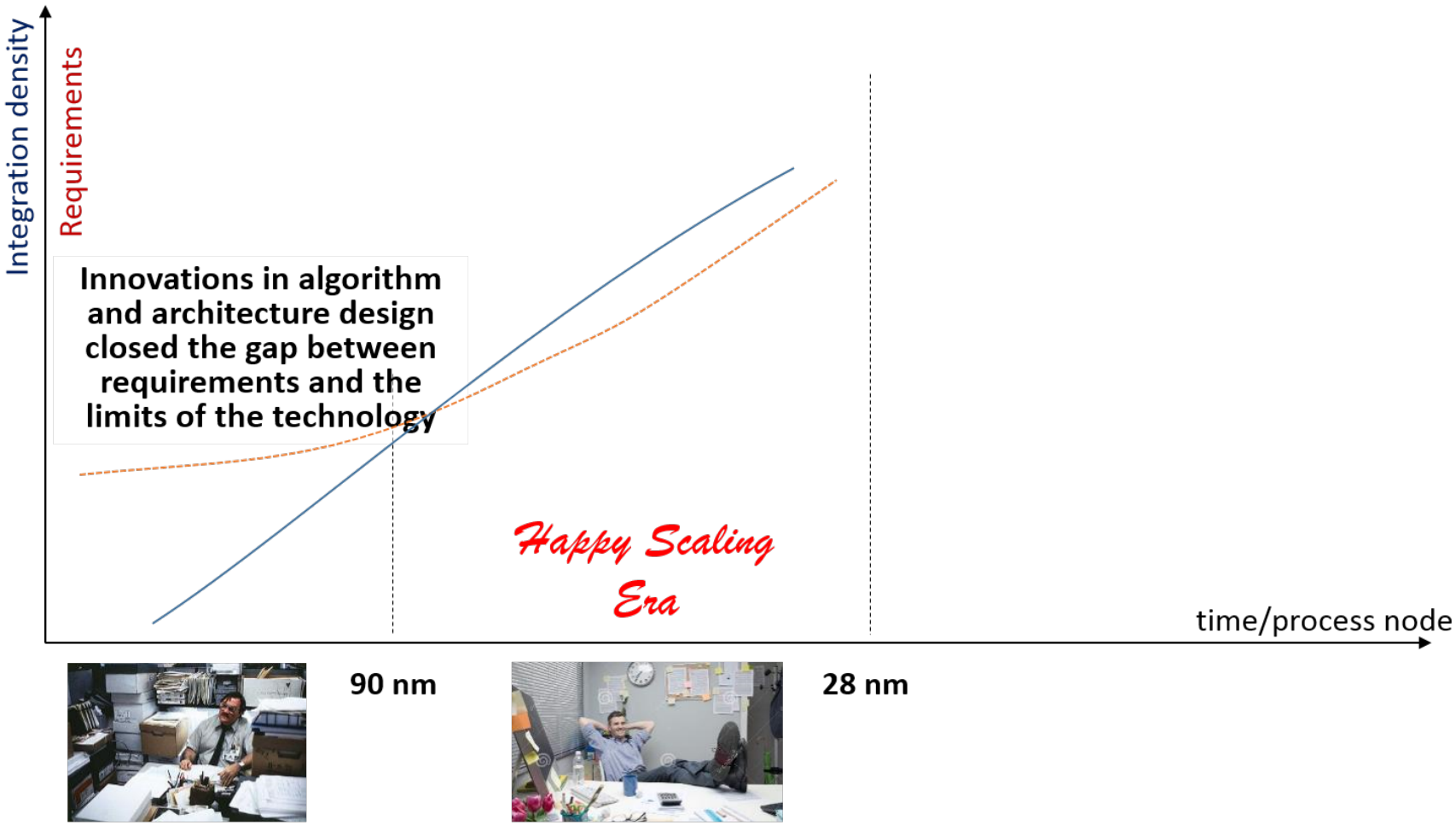
1999: re-discovered by MacKay and Neal

- VLSI technology allowed for the implementation of LDPC codes

Today: LDPC codes are optional or mandatory in almost all standards

- Increasingly favored over other codes for high throughput.

The Dawn of the Happy Scaling Era



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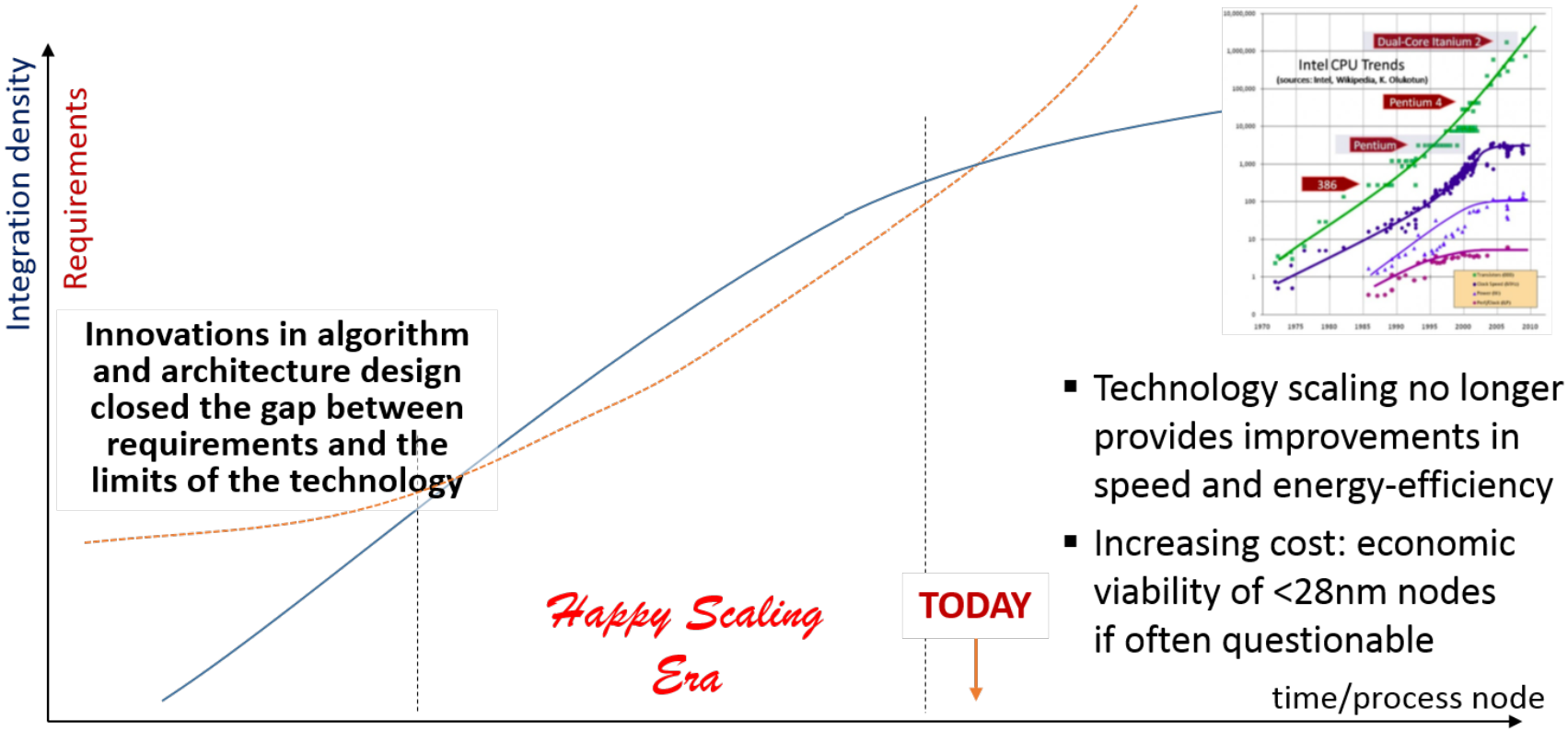


- Technology scaling no longer provides improvements in speed and energy-efficiency
- Increasing cost: economic viability of <28nm nodes if often questionable

The Offset Min-Sum (MS) Algorithm

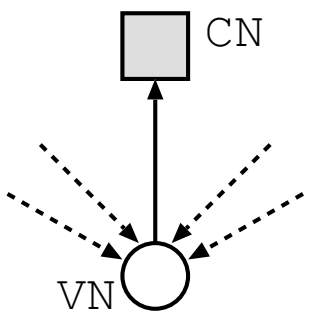
The Min-Sum algorithm and its variants are the workhorses of LDPC decoding.

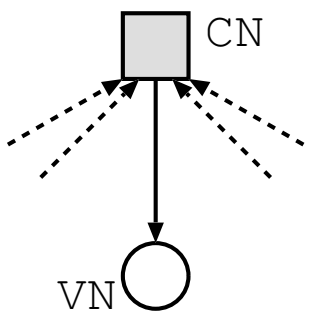
Initialization: Set L_v^0 based on LLRs from the demodulator and set $R_{c,v}^0 = 0$
Iterations: $i = 1 \dots I_{\max}$

$$\text{VN}: \quad Q_{v,c}^i = L_v^0 + \sum_{c' \in \mathcal{N}(v) \setminus c} R_{c',v}^{i-1}$$

$$\text{CN}: \quad R_{c,v}^i = \max\left(\min_{v' \in \mathcal{M}(c) \setminus v} \left(|Q_{v',c}| \right) - \beta, 0 \right) \prod_{v' \in \mathcal{M}(c) \setminus v} \operatorname{sign}\left(Q_{v',c}^i \right)$$

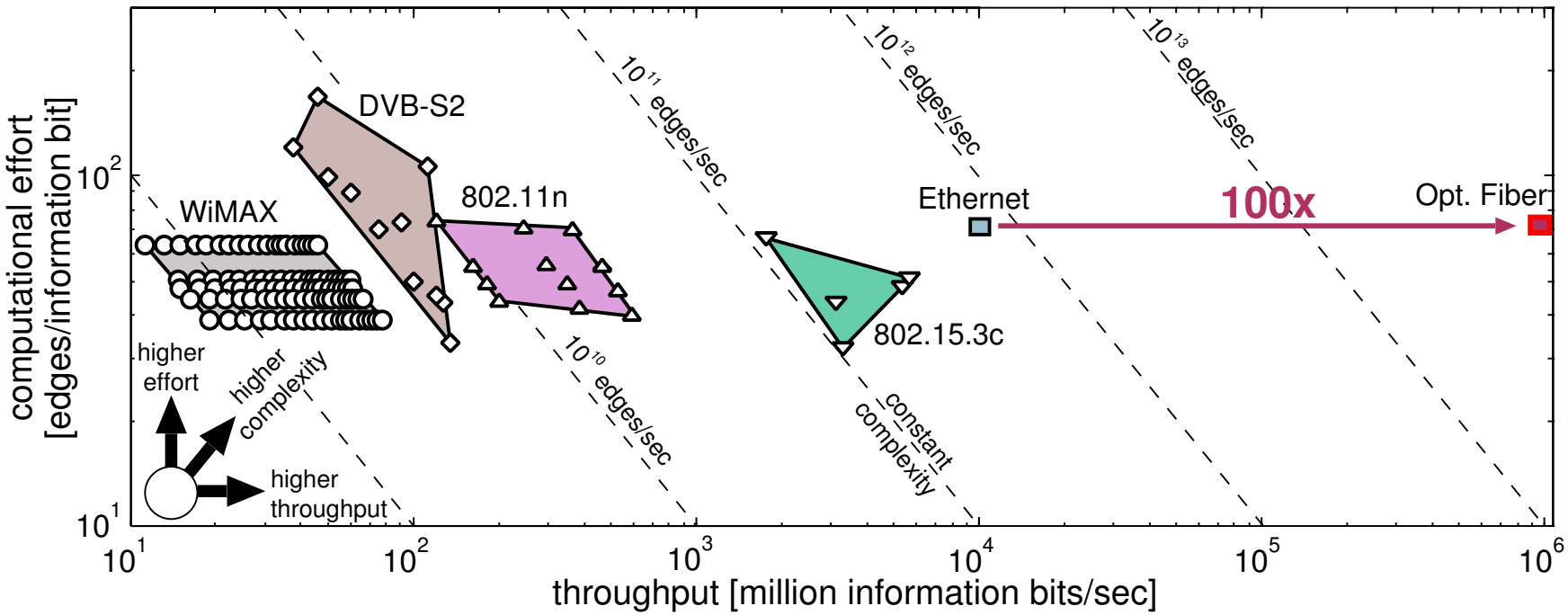
$$\text{VN}: \quad L_v^i = L_v^0 + \sum_{c' \in \mathcal{N}(v)} R_{c',v}^i$$





Computational Complexity of LDPC Decoding

Consider the **computational effort per information bit** and the **required throughput** for different standards and for their different operating modes



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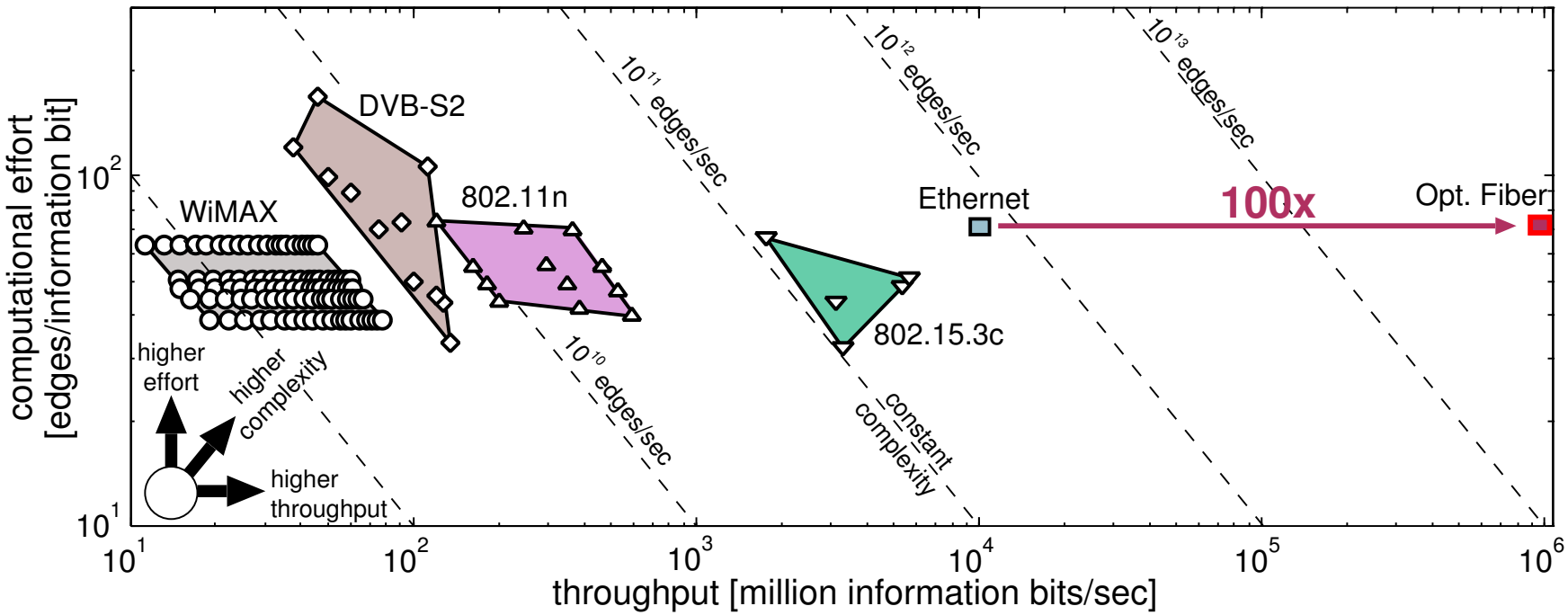
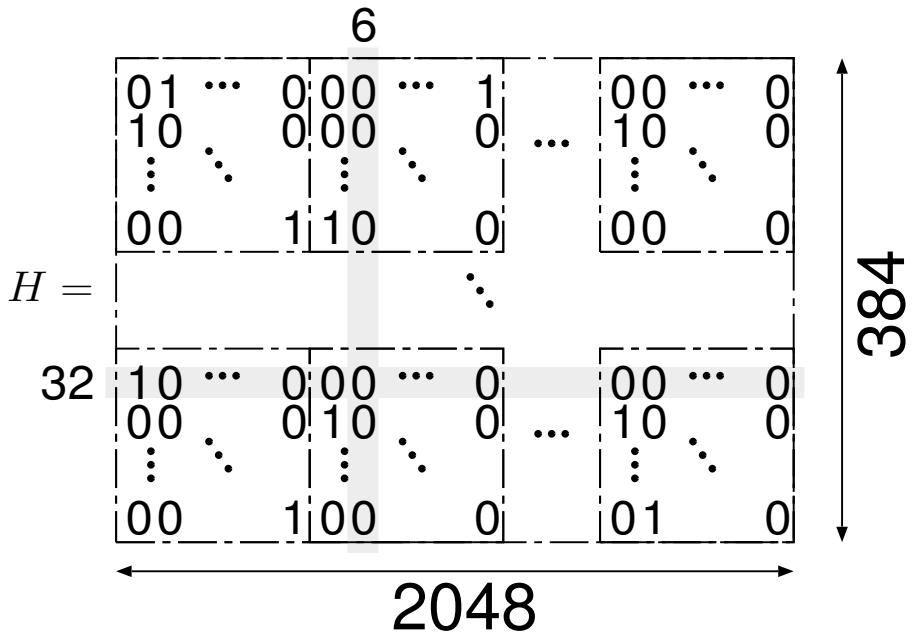


VLSI architectures for LDPC decoding must **cover** more than **6 orders of magnitude in throughput** and **different degrees of reconfigurability**

10GBASE-T 10 Gbps Ethernet

10GBASE-T employs a (6,32)-regular (2048,1723) code with rate $R = 0.84$

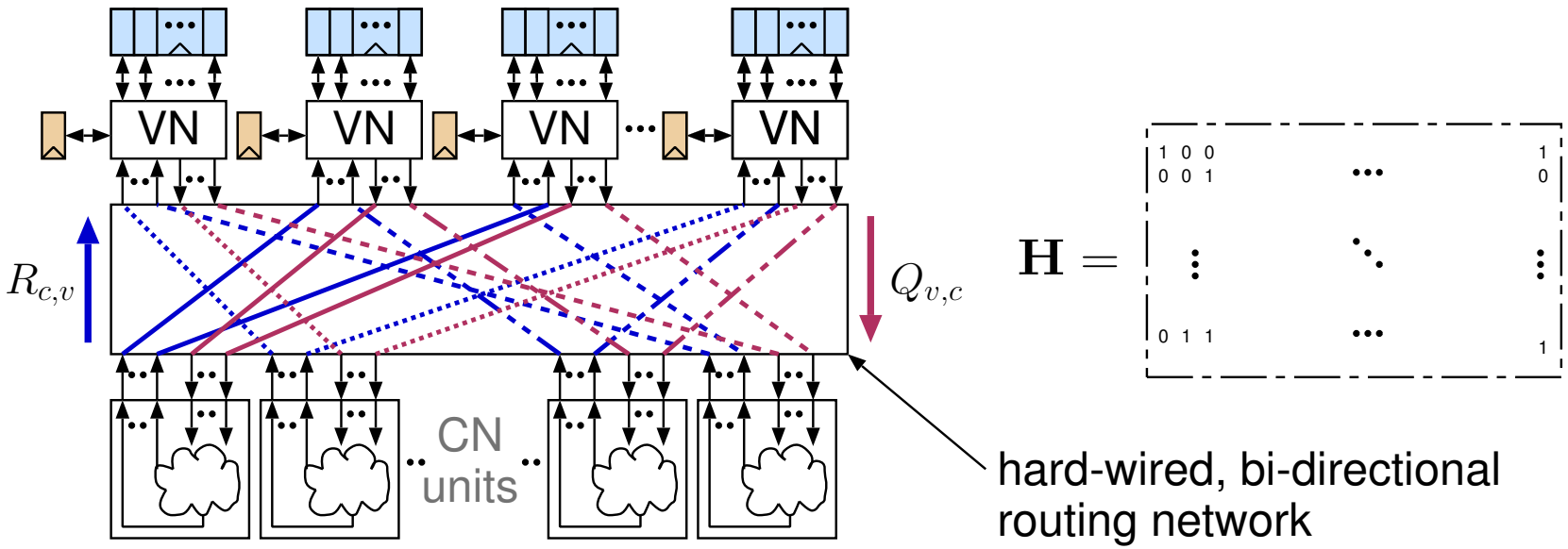


- 384 Check Nodes, 2048 Variable Nodes
- Organized in 6 layers
- 12'288 edges in the corresponding Tanner graph

Fully Parallel Implementation

Isomorphic architecture: direct mapping of Tanner graph onto silicon

- Instantiate **2048 VNs** and **384 check nodes**
- **Edges** are implemented through a global routing network
- **Each iteration** is carried out in **one cycle**



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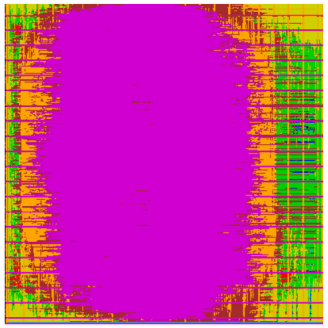
- Throughput: 1.7 Gbps
- Silicon area: 18.2 mm^2
- **Core utilization: 25%**



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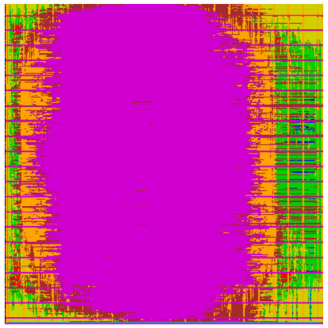

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The **exchange of messages** between VNs and CNs requires **more than 100'000 global point-to-point connections**

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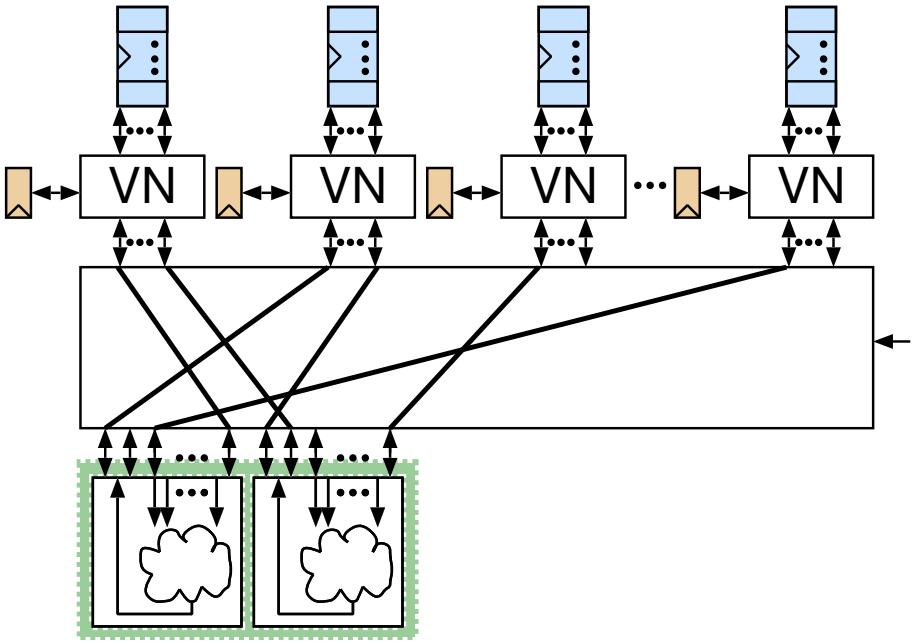
Layered decoding: Modify the schedule of VN and CN operations

- Process **one layer at a time**, but **update VNs after each layer**



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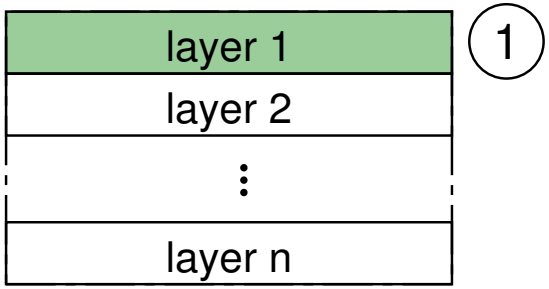

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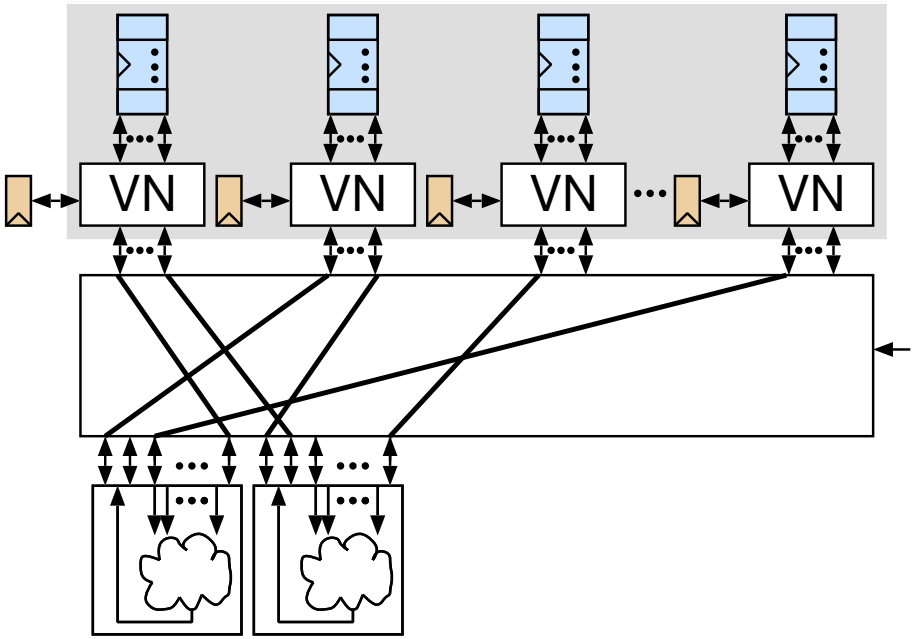

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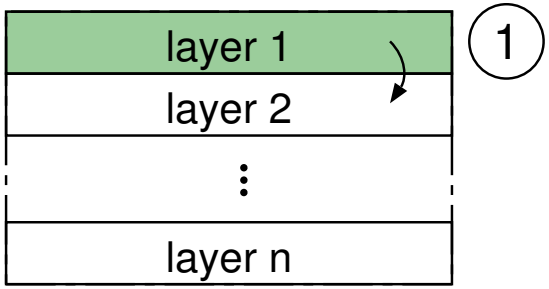

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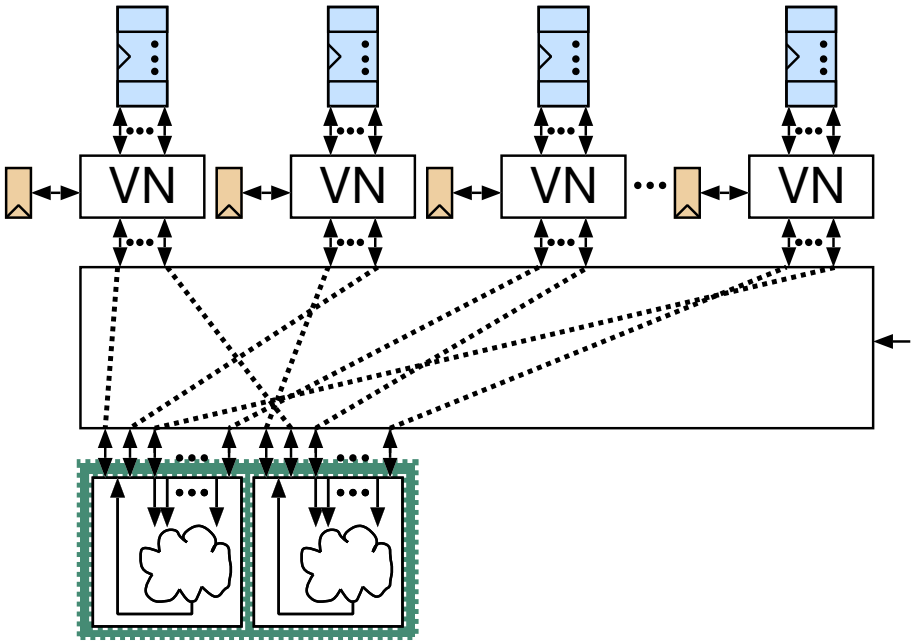

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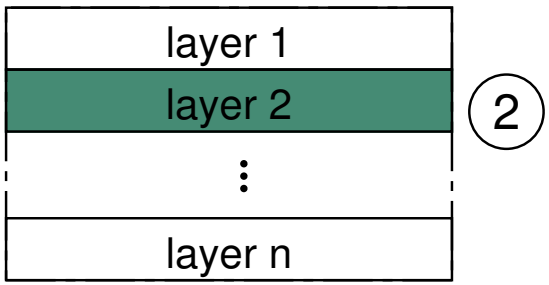

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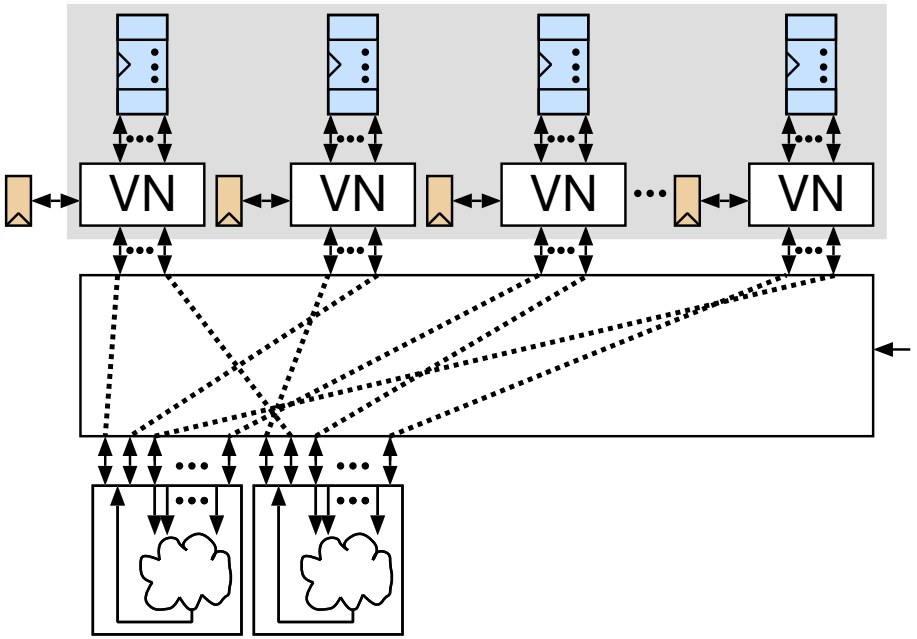

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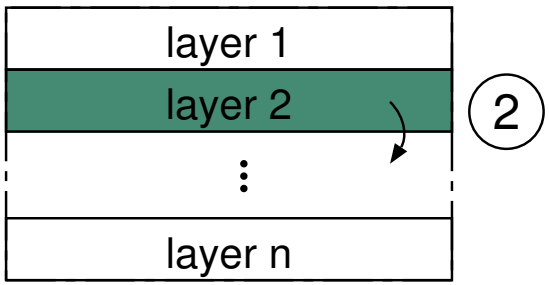

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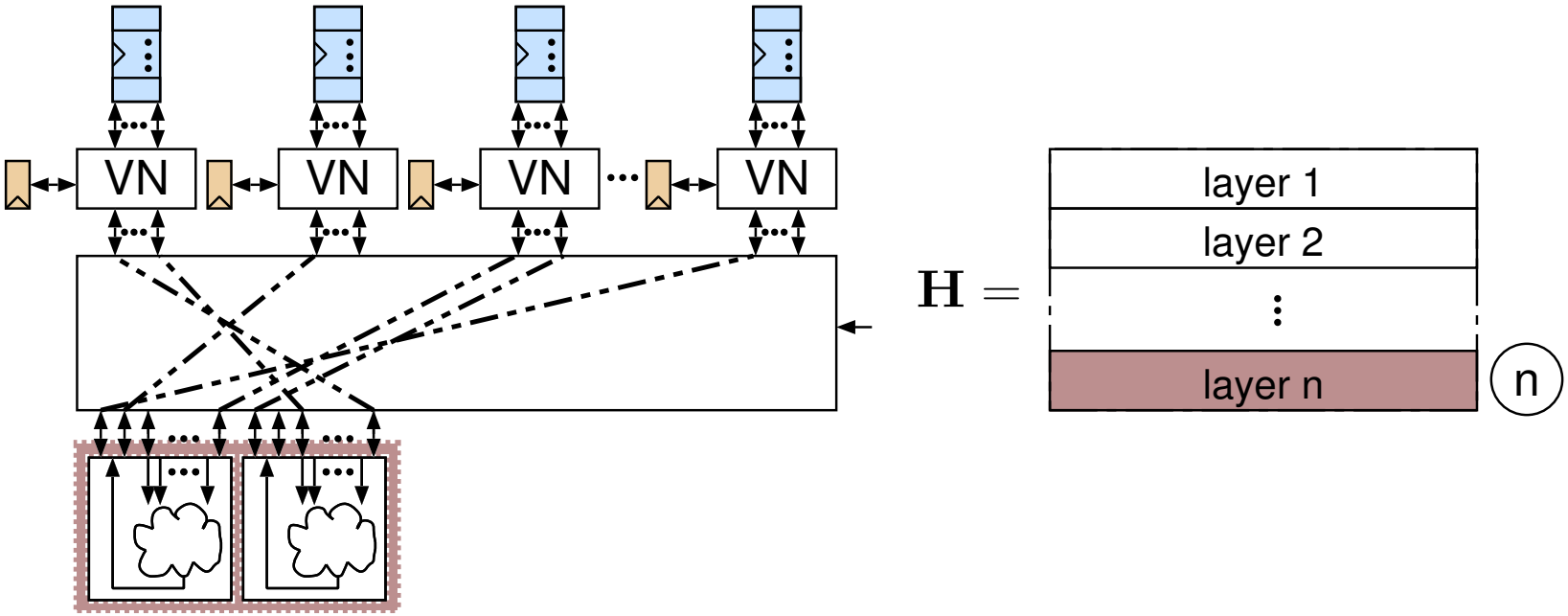

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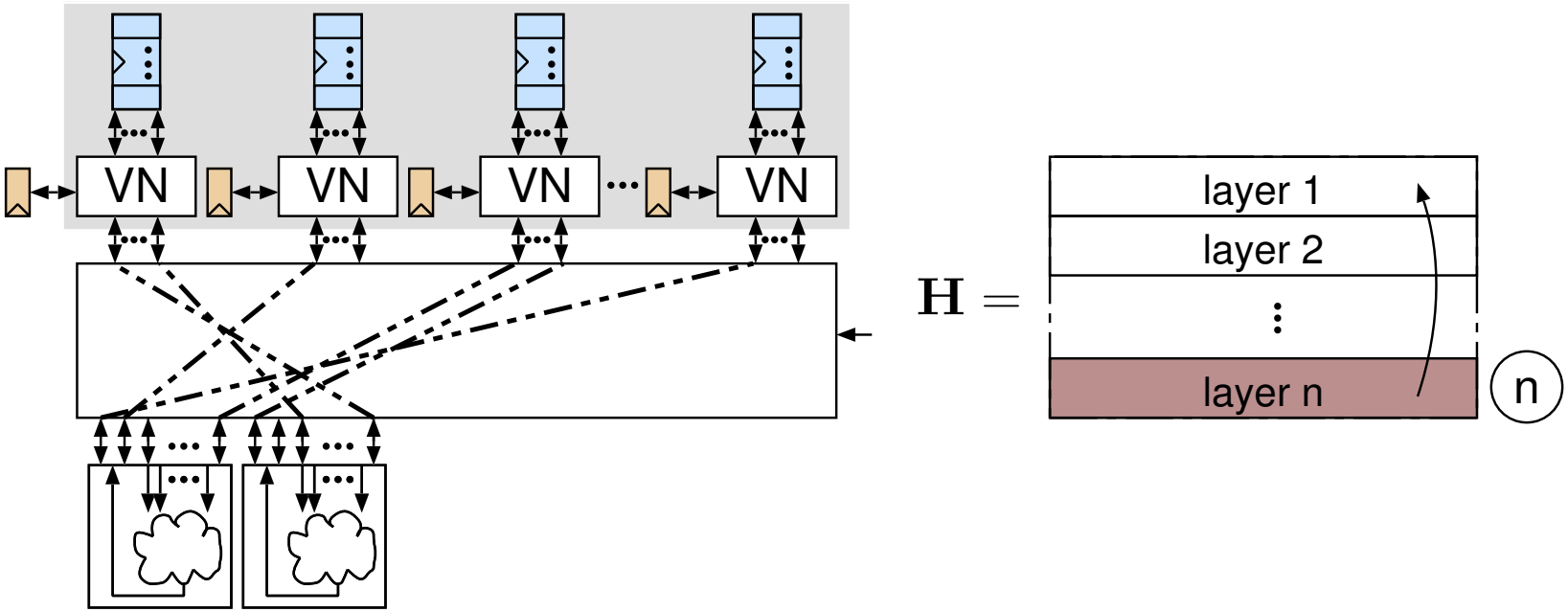

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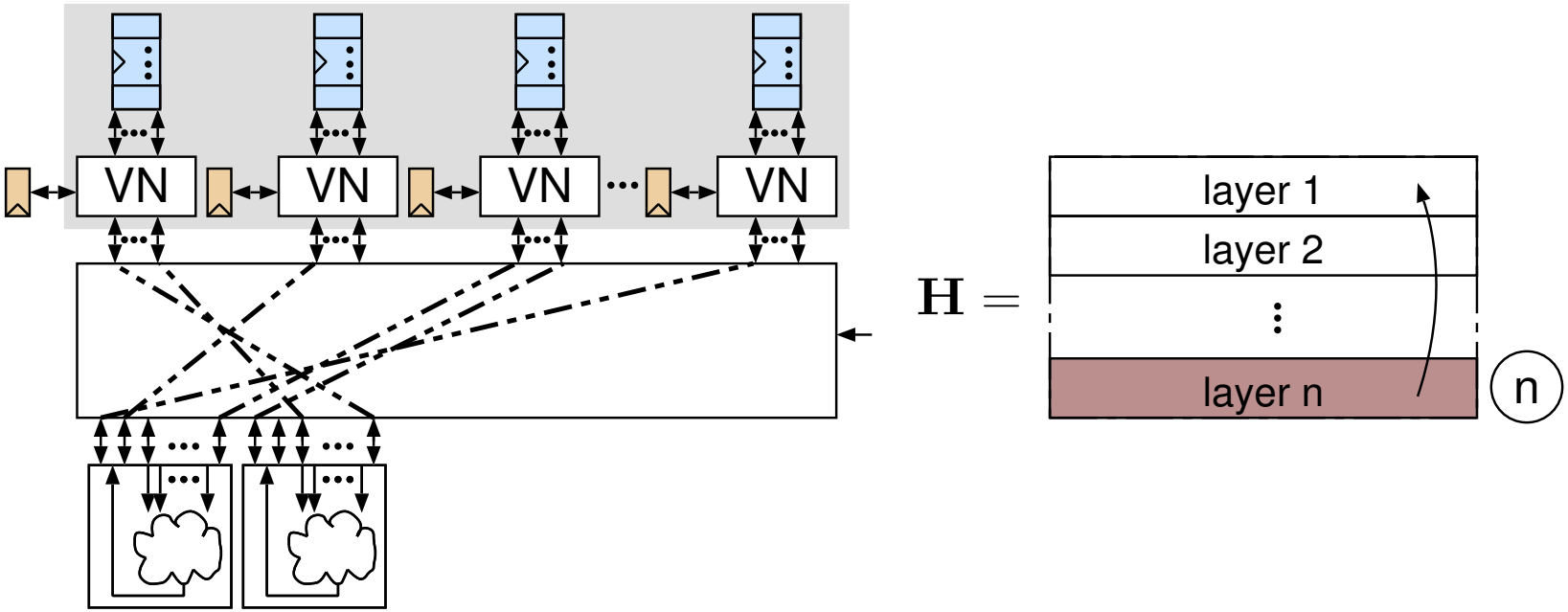
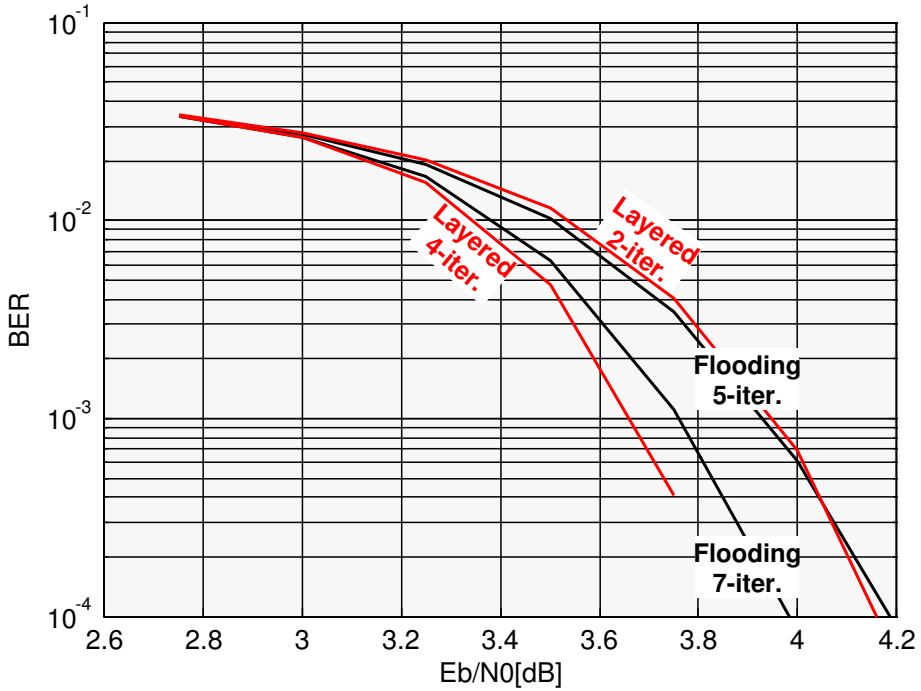


Layered decoding enables efficient time sharing of resources

Impact of Layered Decoding on Performance

Using a **layered schedule** results in a behavior that is **different from** message passing with a **flooding schedule**



BPSK, AWGN, (2048,1723) LDPC code for 10GBASE-T with OMS decoding, $\beta = 1.0$

The **layered schedule improves convergence**

↓

Reduces throughput loss from resource sharing.

Solving the Routing Issue with Circuit Techniques

Main issue: Routing overhead is one of the main limitations (density & frequency)

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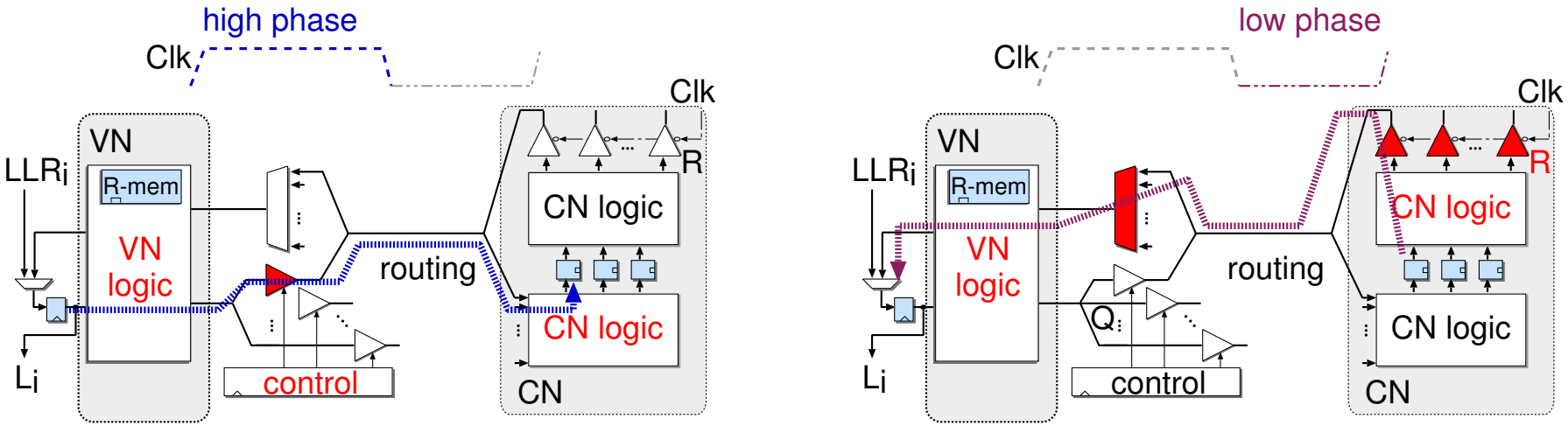
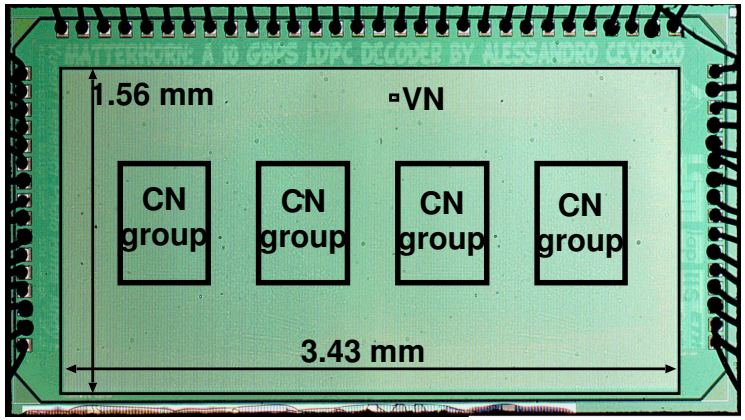
Solution: Time share routing wired for VN→CN and CN→VN routing



Full-duplex routing

Enables 50% less routing wires and enables 84% area utilization

10 Gbps LDPC Implementation Results



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Tech. [nm]	90	65	65	90
Algorithm	OMS	OMS	split-row-16	SPA
Scheduling	layered	flooding	flooding	flooding
Area [mm^2]	5.35	5.35	3.8	14.5
Speed [Gb/s]	**11.69**	**13.3**	**13.8**	5.30
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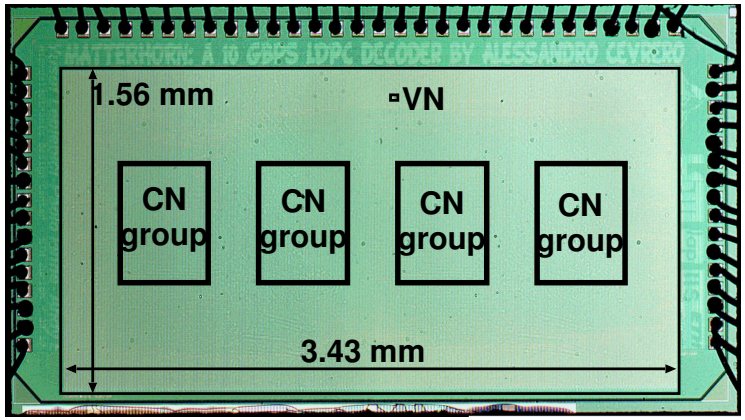

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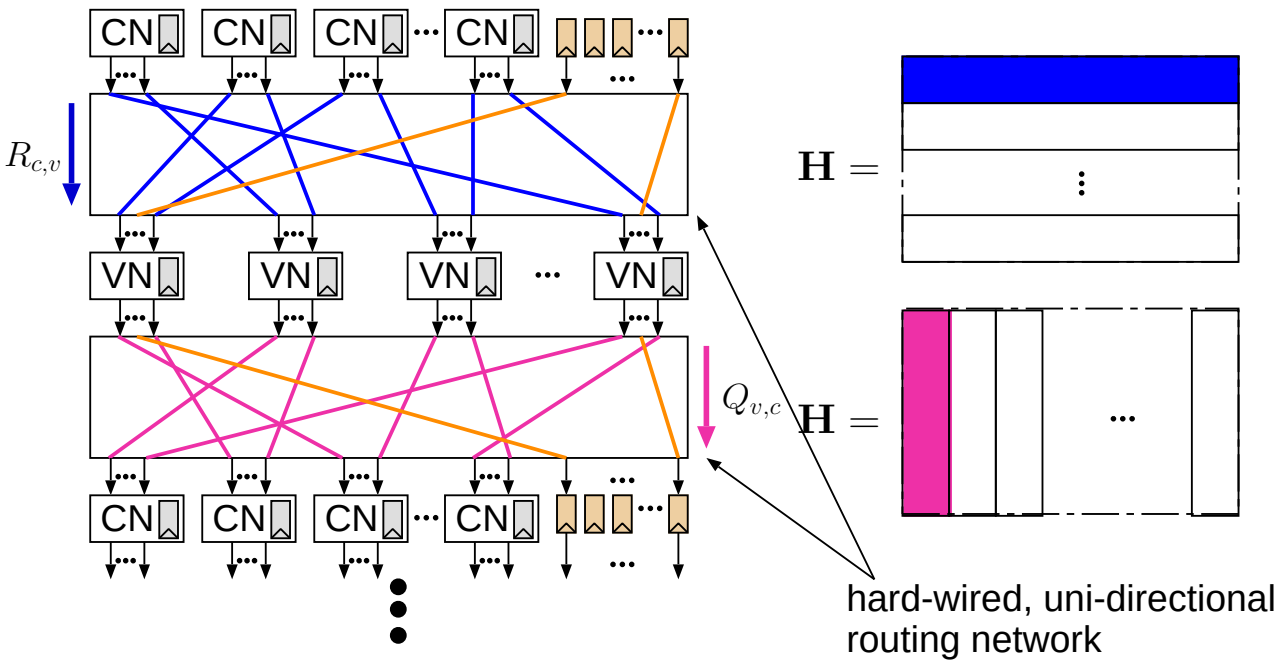
Throughput scaling beyond 10 Gbps limited by sequential processing and routing overhead which limits frequency.

Unrolled Fully Parallel Implementation

Unrolled architecture: mapping of all decoding iterations onto silicon

- **Each iteration** is instantiation of **2048 VNs** and **384 CNs** (two stages)
- Decoder architecture consists of **distinct sets** of VN and CN stages **for each iteration**
- **Connections** are realized through routing networks between CN/VN stages
- **One decoded codeword per cycle**



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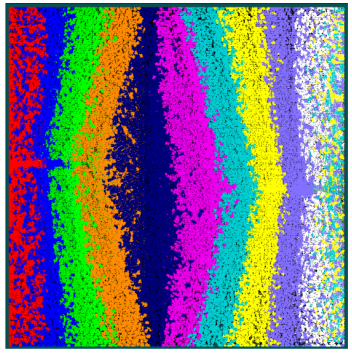

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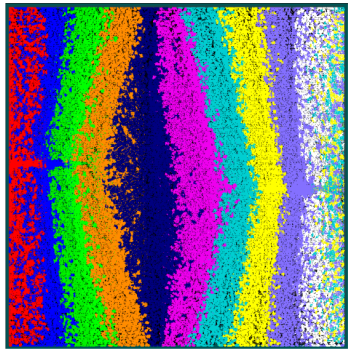

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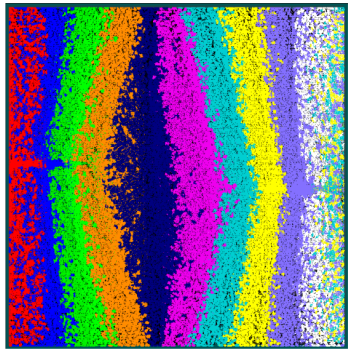

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More complex codes require further reduction of the routing congestion.

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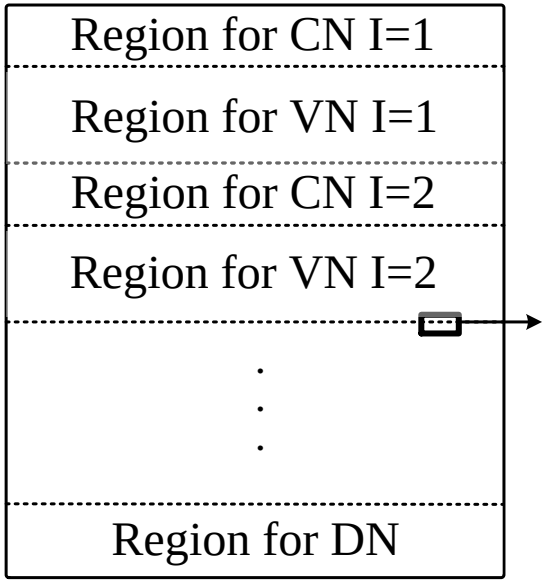

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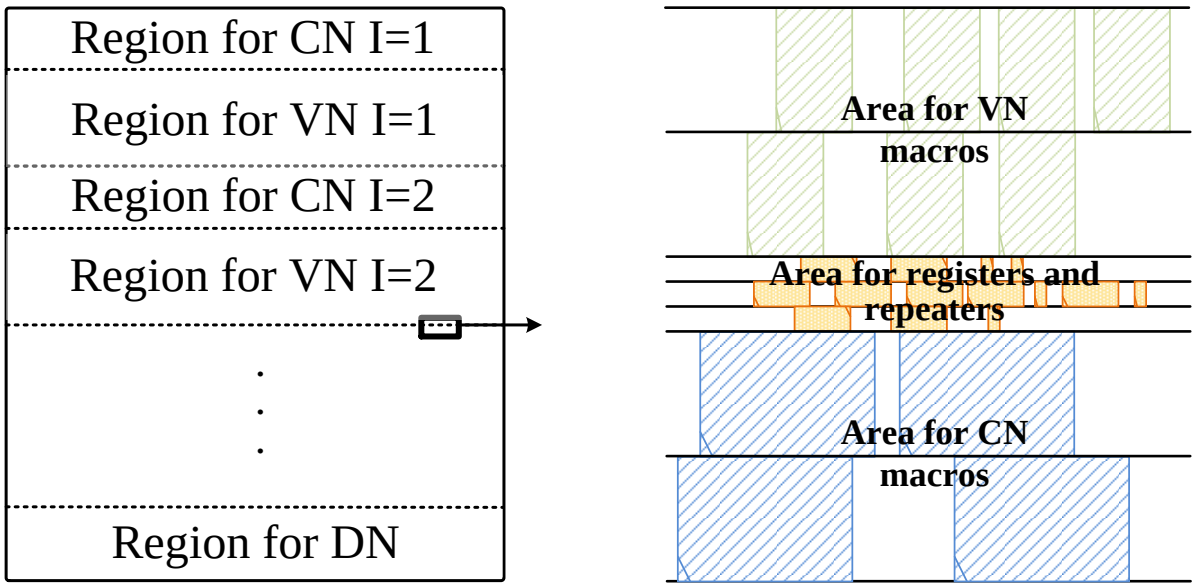

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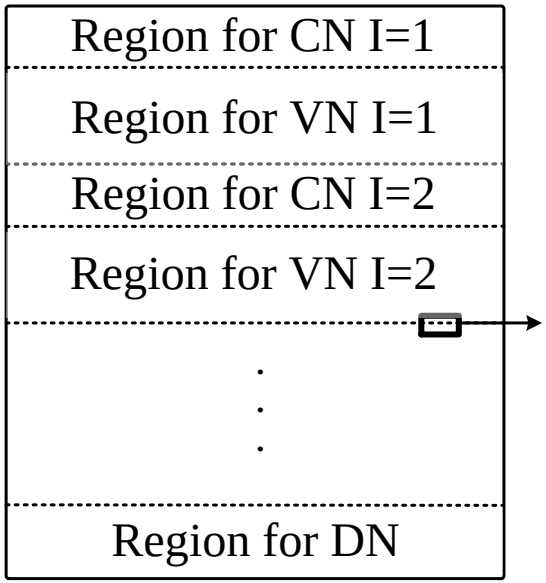

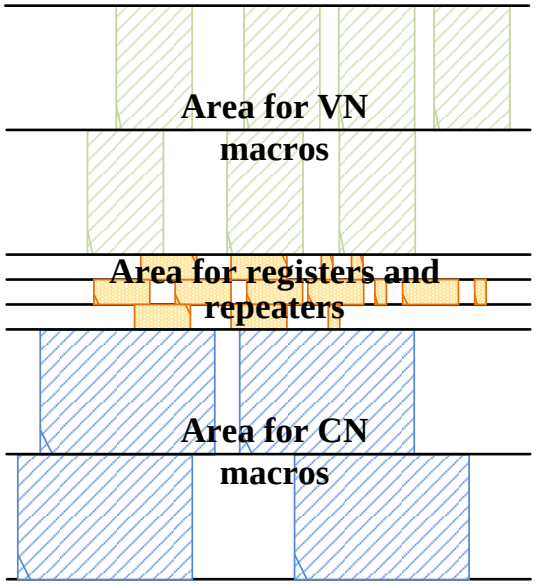

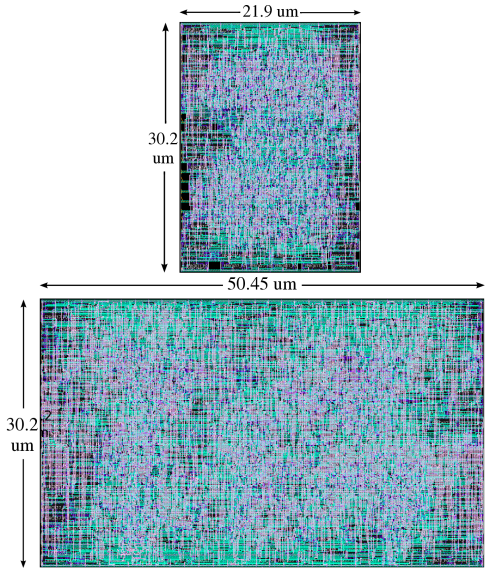

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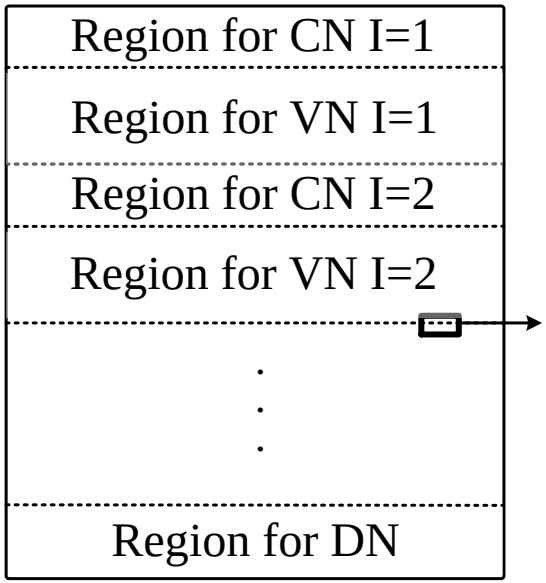

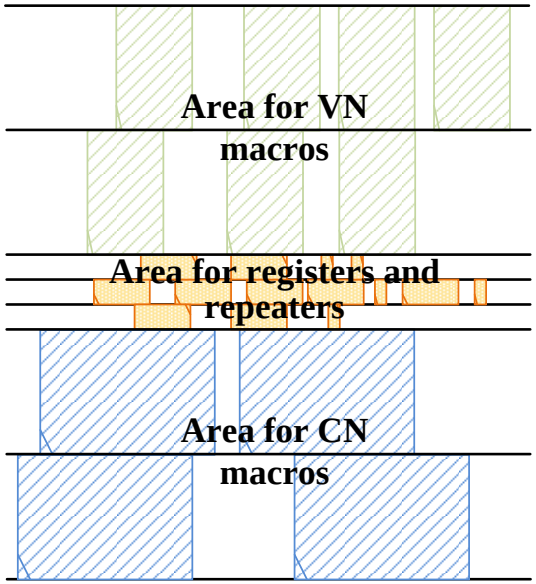

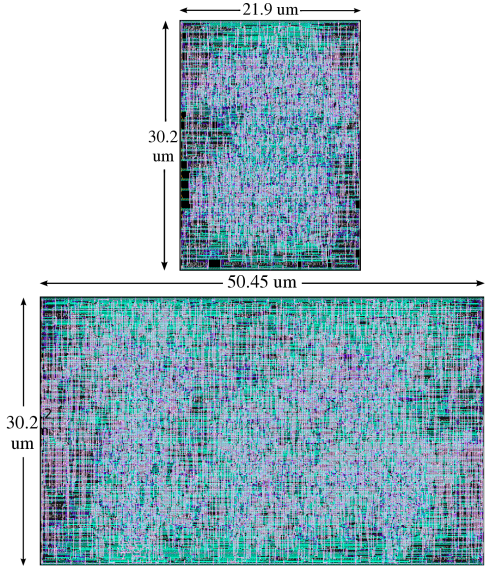

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Even with structured layout, **routing overhead remains prohibitive**

Serial Message-Transfer Architecture

Main idea: Send/receive messages serially.

- Transfer each message bit-by-bit through a single wire
- Overlap (pipeline) message transfer with processing
- Process two codewords interleaved
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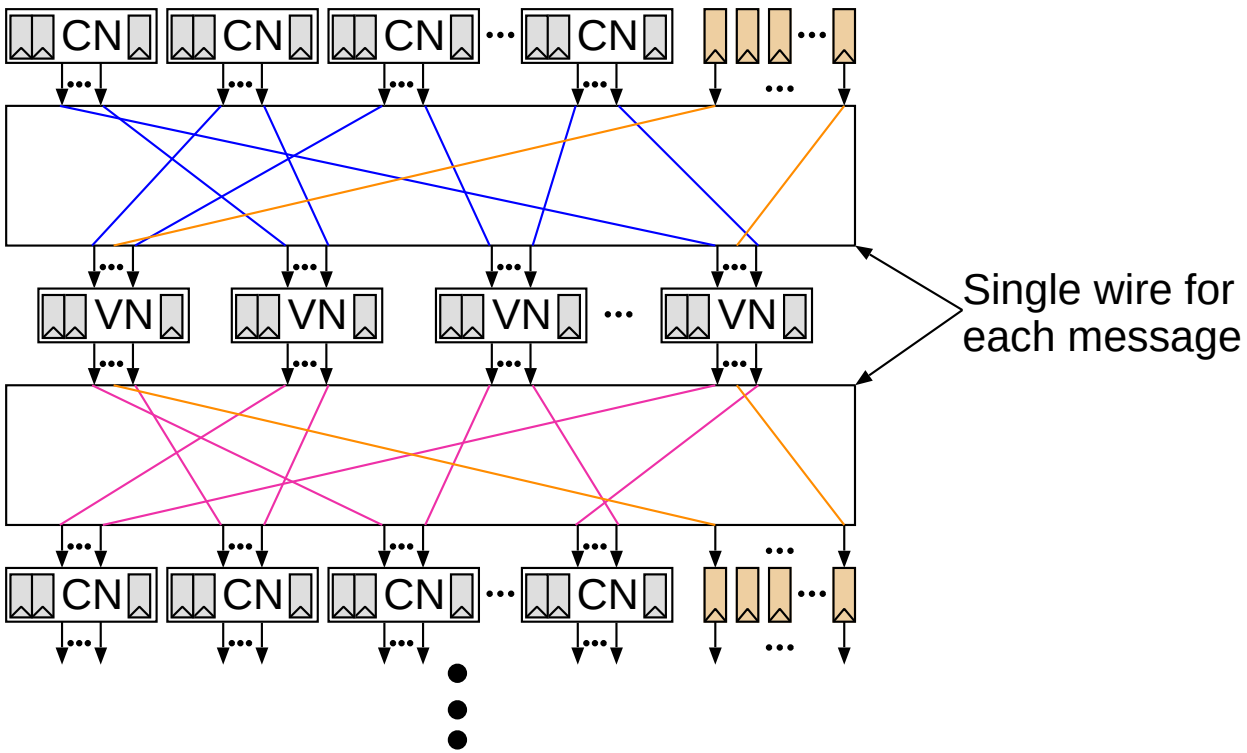

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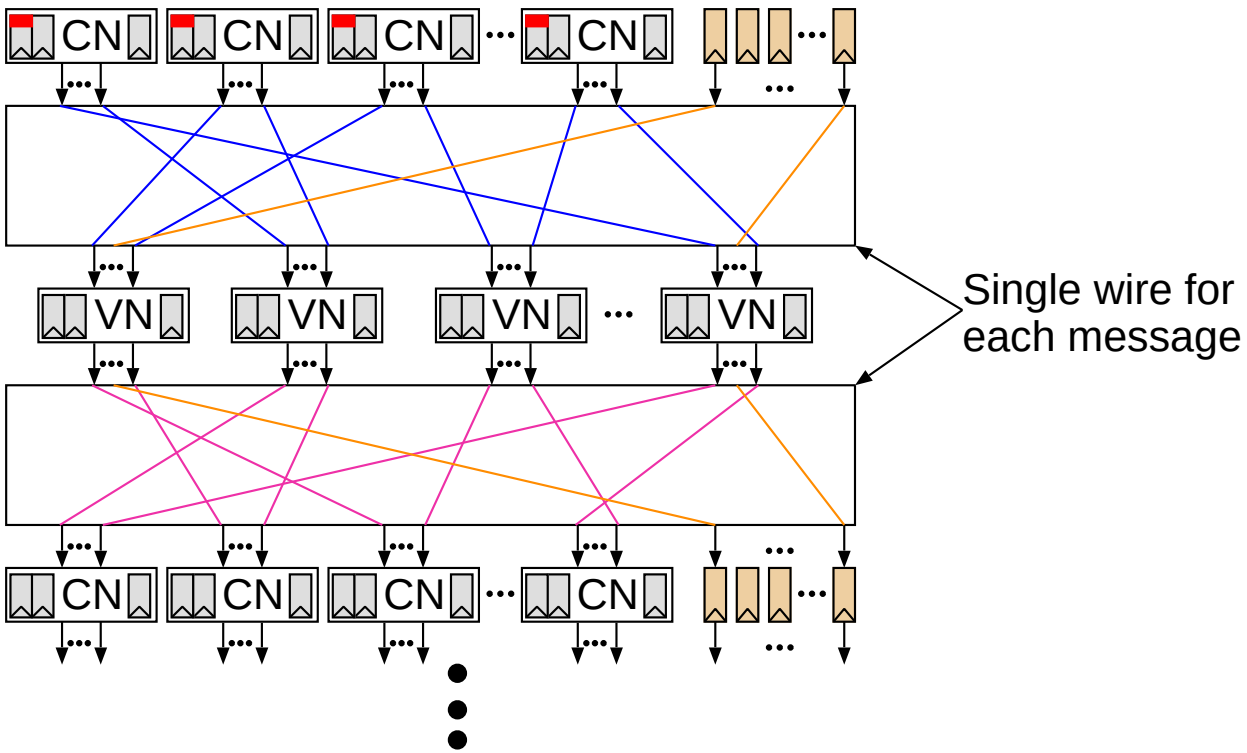

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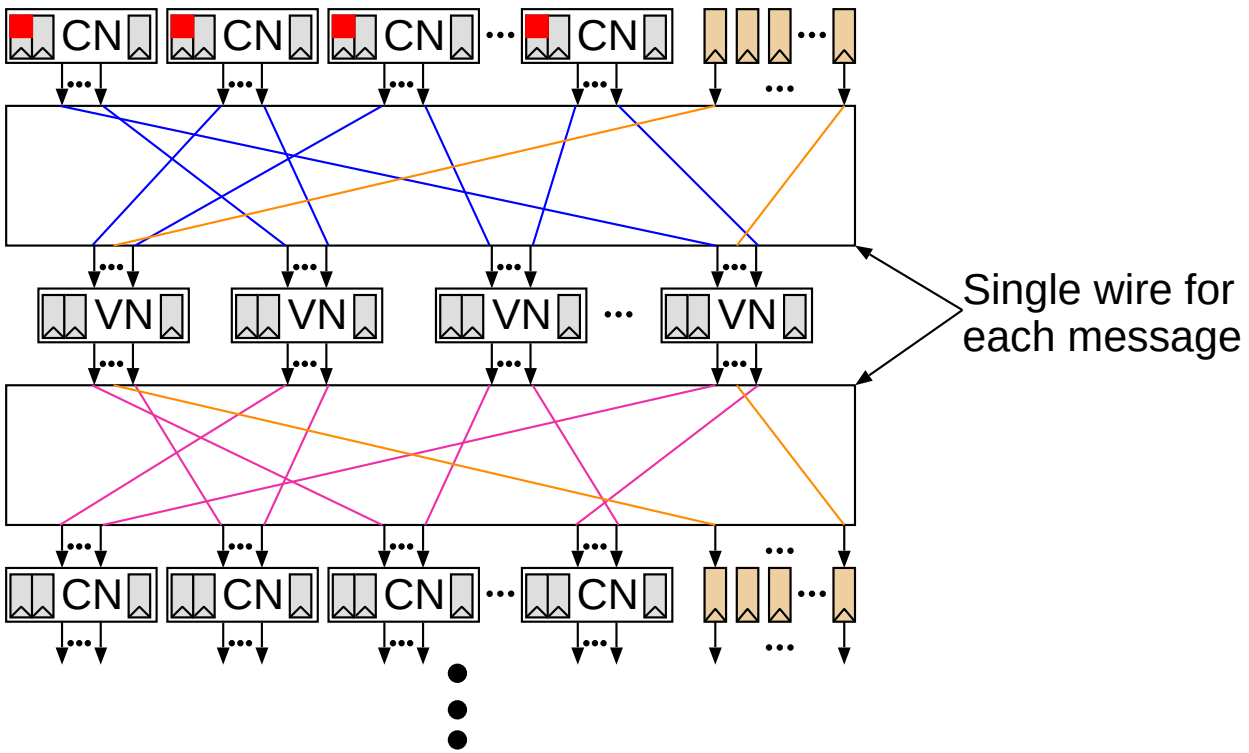

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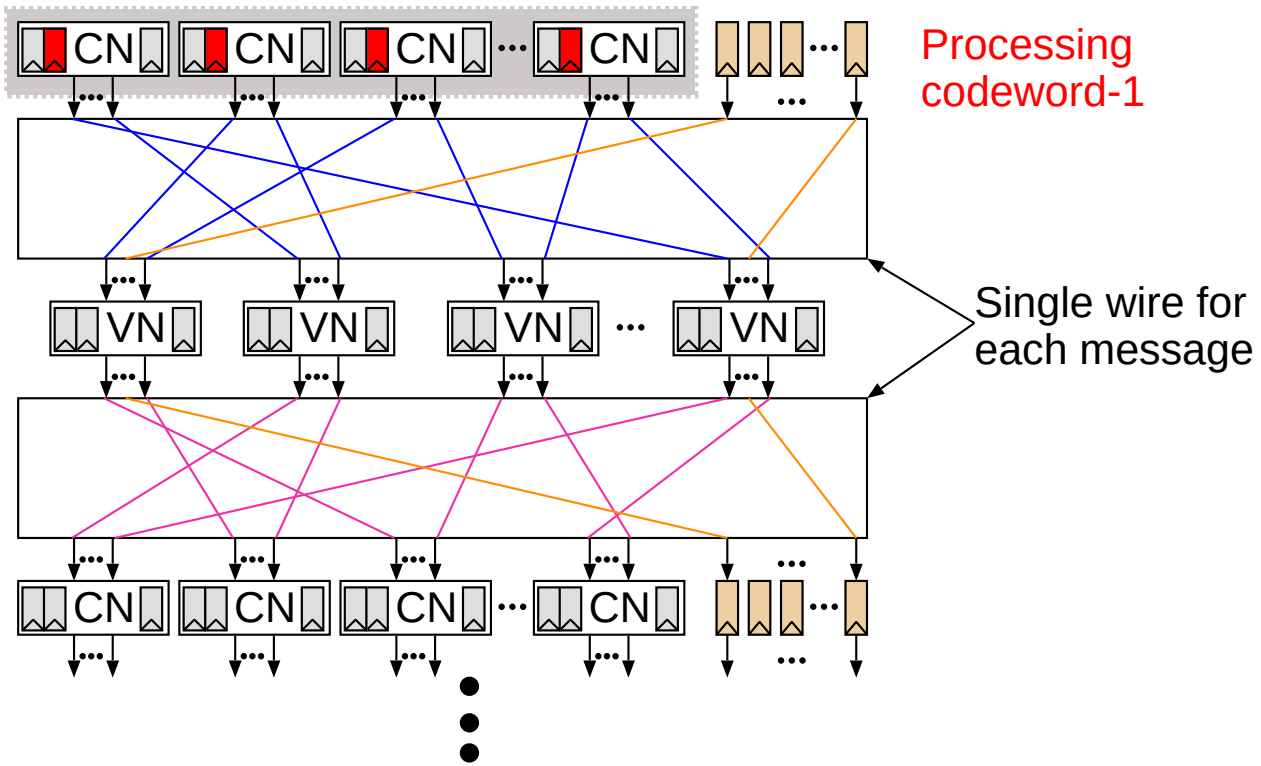

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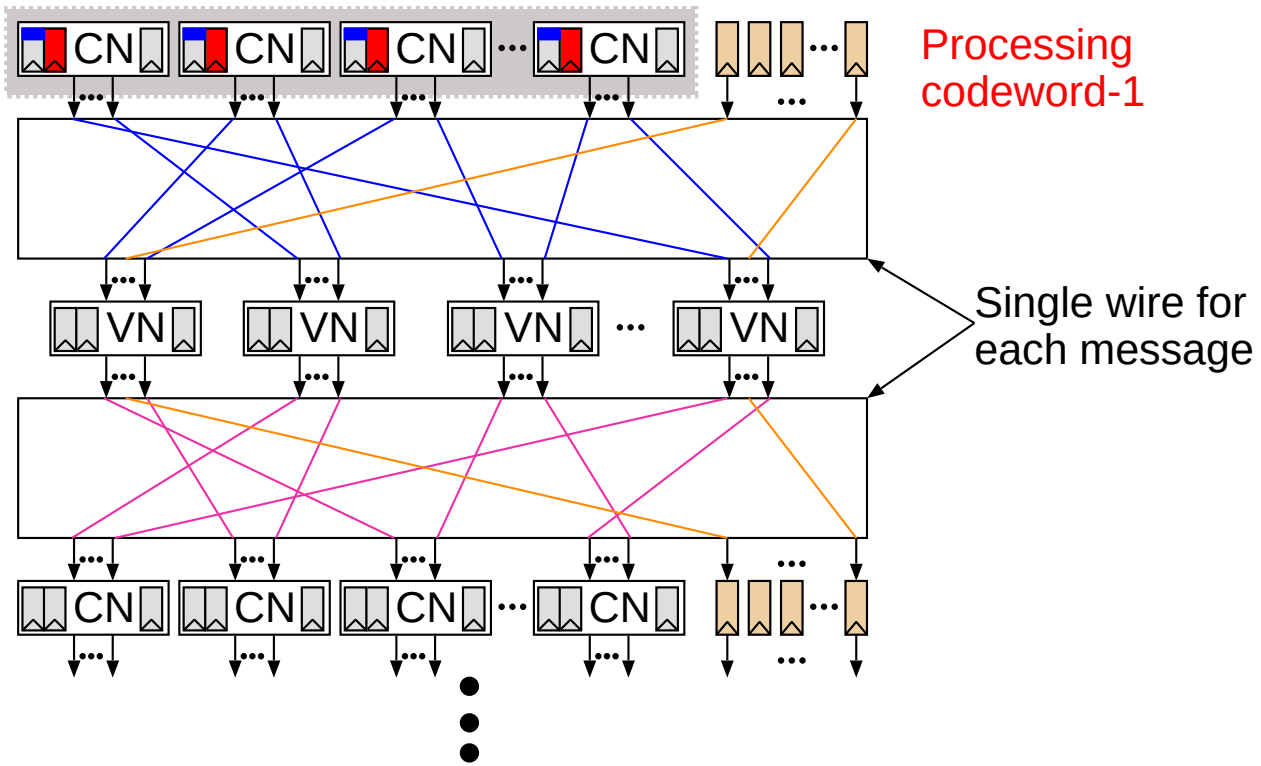

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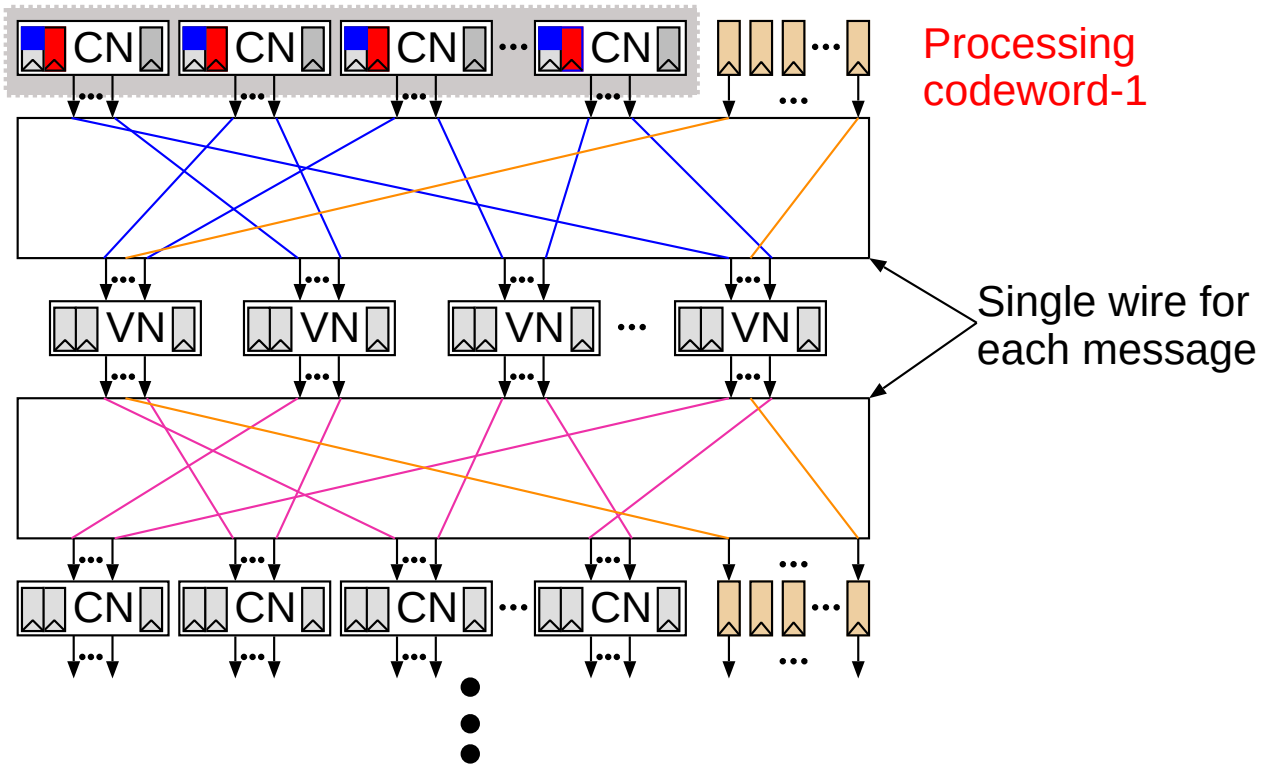

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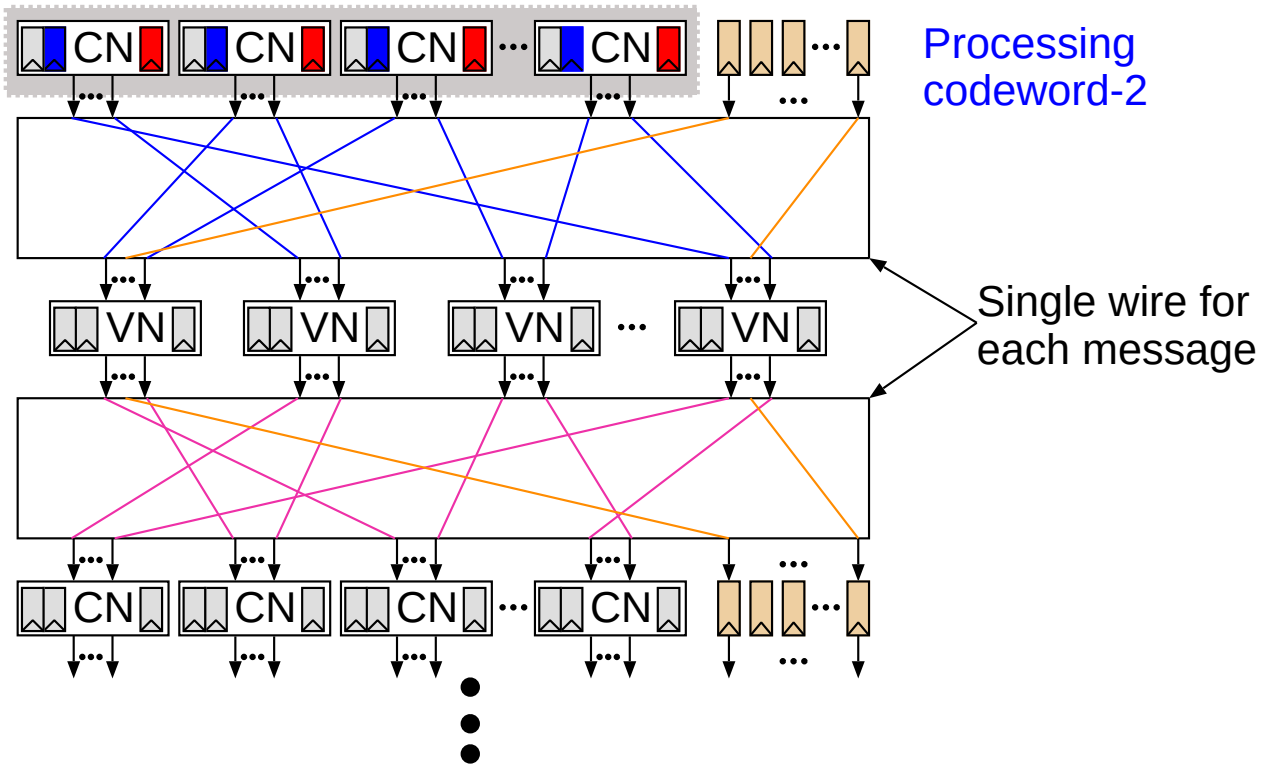

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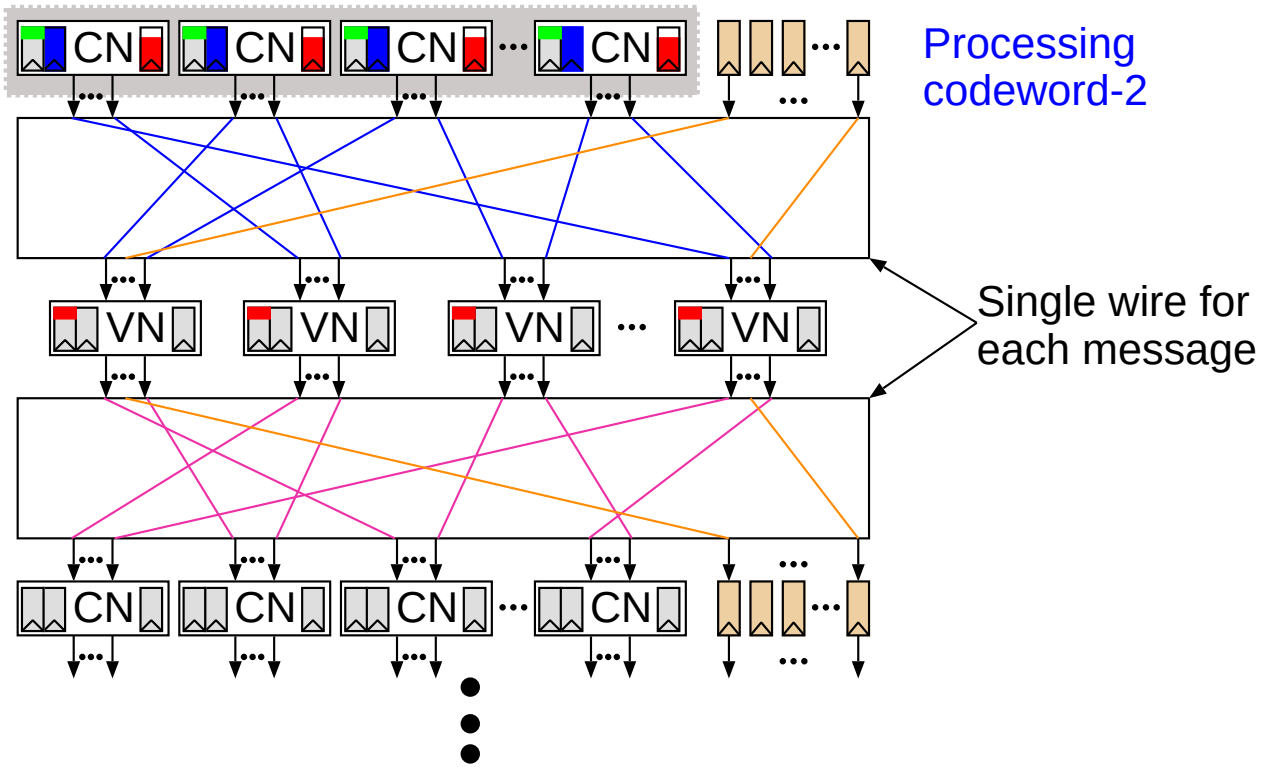

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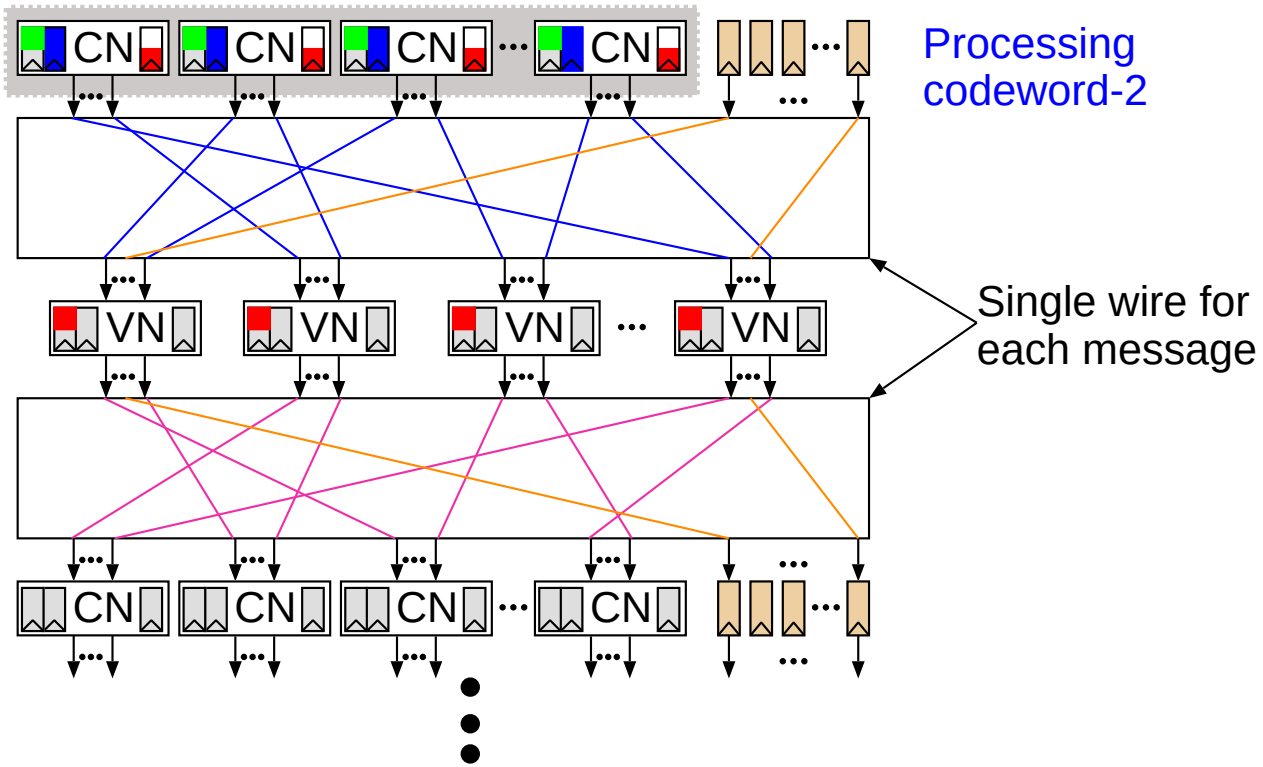

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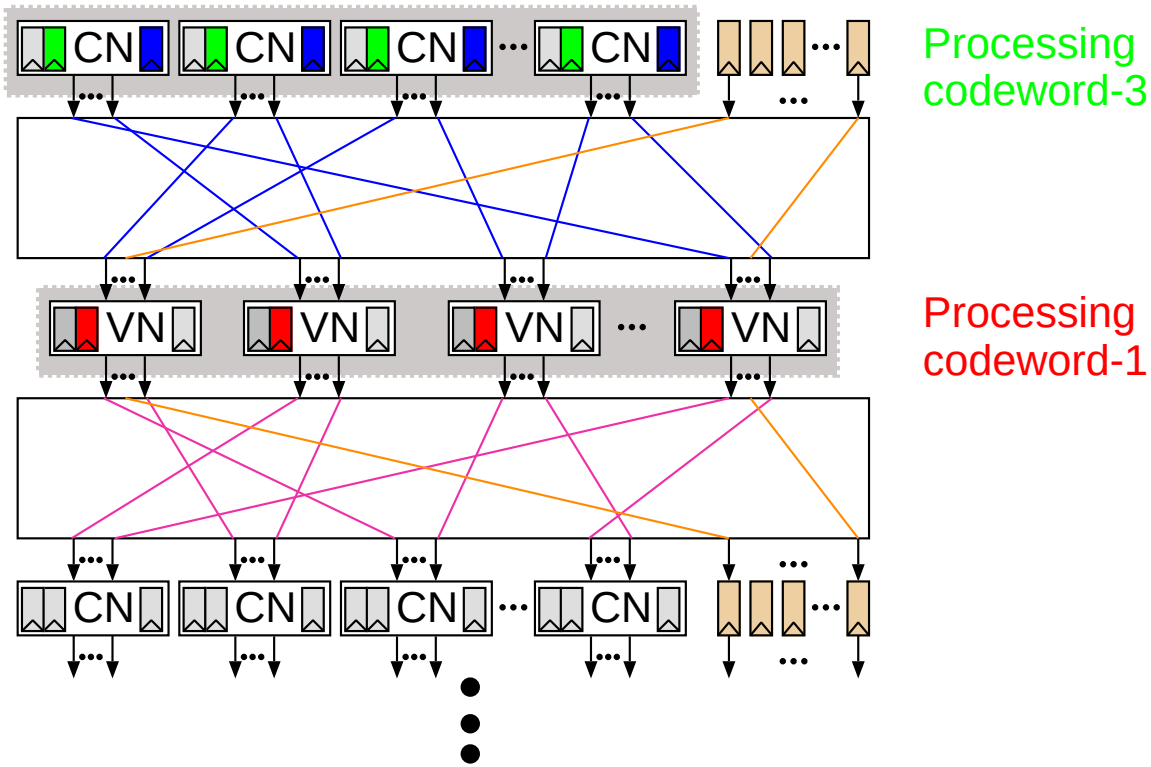


Serial Message-Transfer: Pros & Cons

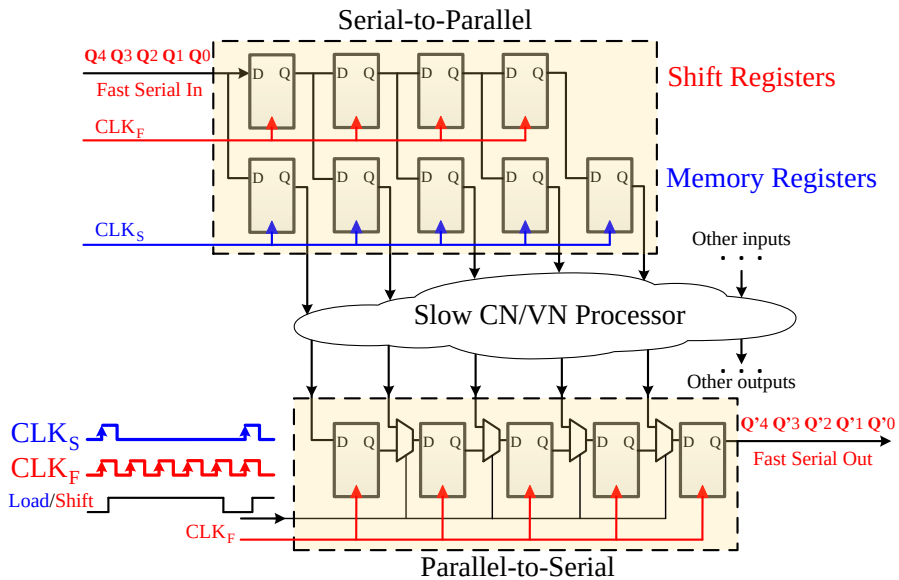
Advantages:

- **Routing congestion is significantly reduced**
- **Overlapped processing** of two codewords **hides message transfer** delay
- Signal **routing in a separate pipeline stage** (no increase in logic delay)

Disadvantages:

- Number of registers increases by 3x
- Decoder latency increases by 2x
- Minimum clock period limited by

$$T_{clk} > \min\left(T_{clk_{logic}}, Q_{msg} \times T_{clk_{routing}}\right)$$

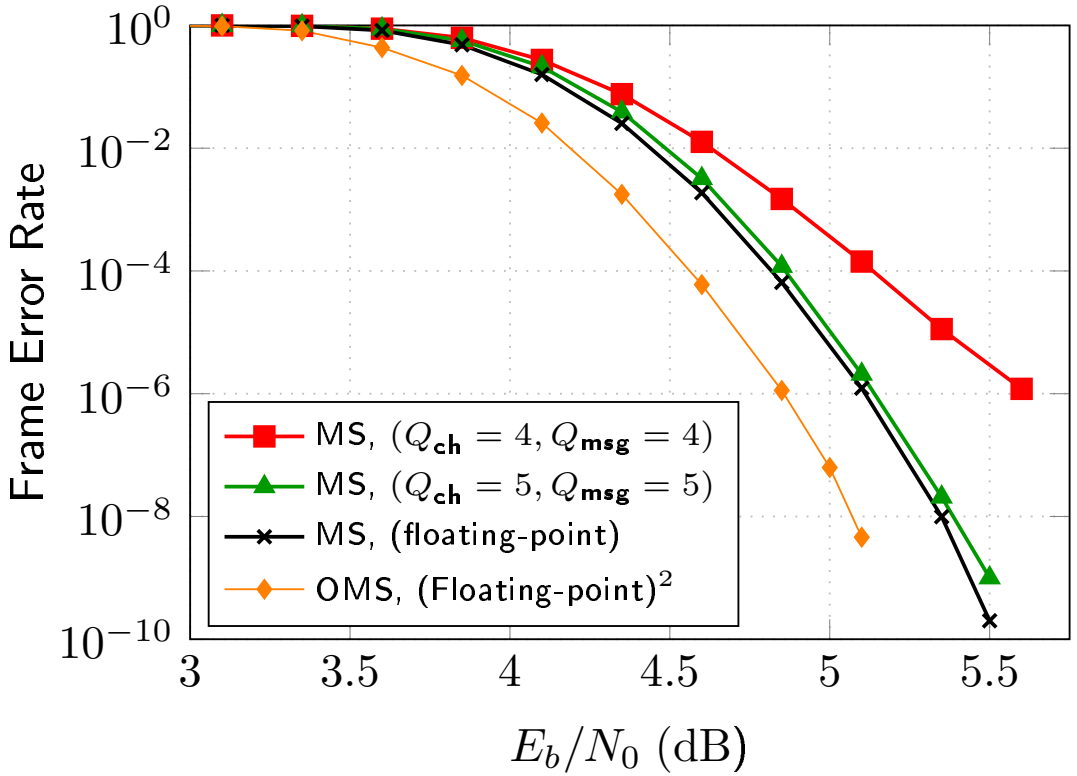


Routing delay must be significantly shorter than logic delay.

Min-Sum Message Quantization

Message quantization (wordlength) Q_{msg} has a critical impact on

- Complexity (area and delay) of VNs and CNs
- Message-routing overhead between stages
- Decoder performance (FER)



Message quantization with $Q_{msg} \geq 5$ bit required.

Unrolled Serial Message-Transfer Results

Example: Quantization of messages with $Q_{msg} = 5$ bit

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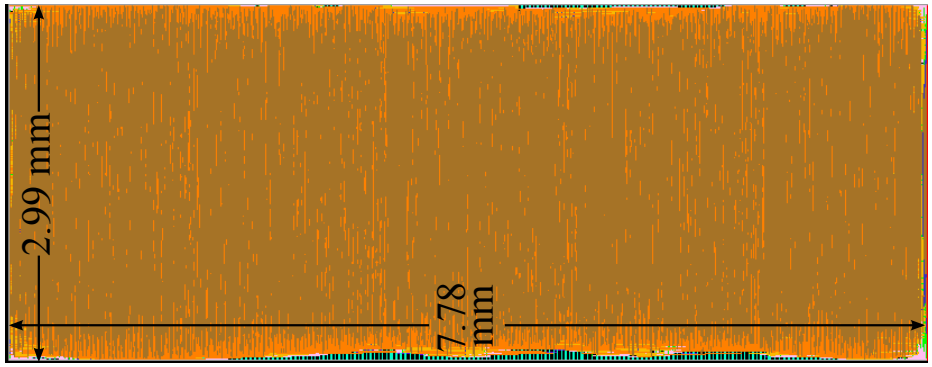

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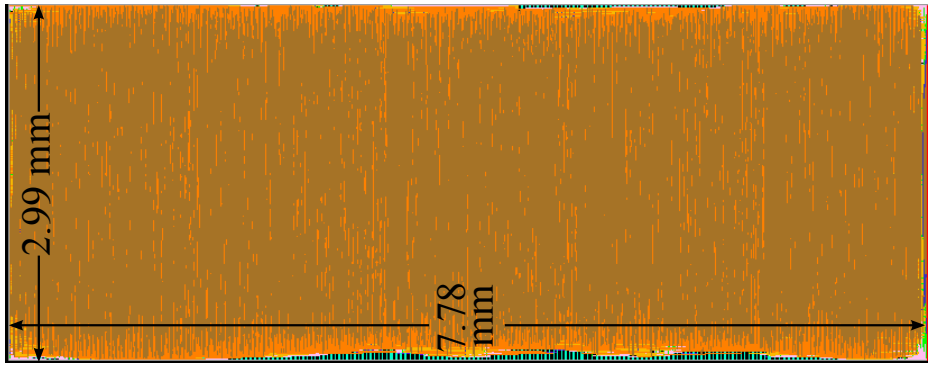

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Throughput: 271 Gbps

- Required time for processing: $T_{logic} = 2.38\,ns$
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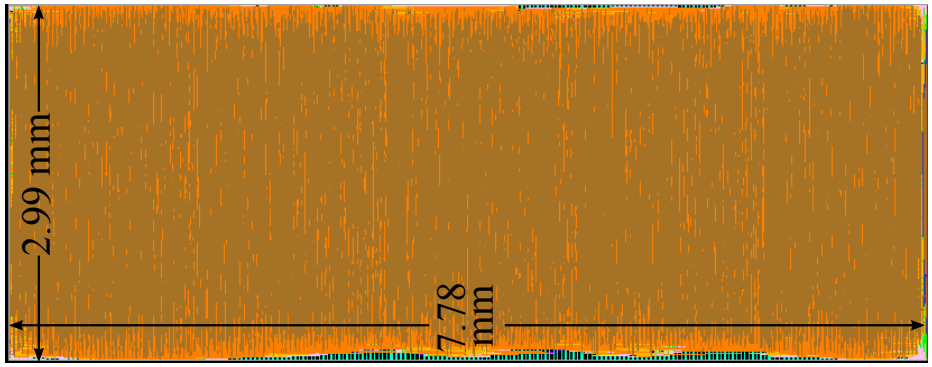

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Decoding throughput is **limited by serial message transfer** of 5 bit messages

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- Update rules must be implemented as general **look-up tables**, which can require **significant area**.

Look-Up Table Design

Numerous LUT design methods [Planjery'13, Declercq'13, Cai'14, Kurkorski'14].

- Our method is similar to Kurkorski'14 and is based on an **information theoretic** criterion (Information Bottleneck (IB)).

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$p_X(x)$ is usually known, but we **need to calculate** $p_{M|X}(m|x)$.

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Use Density Evolution to compute message probability-mass function:

- CN output messages:

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- Check node LUTs can be designed similarly. Due to complexity issues, in this work, **we only examine LUT-based VNs for regular LDPC codes**.

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LUT design **depends on channel LLR distribution** $p_{\mathsf{L}|\mathsf{x}}(L|x_0)$.

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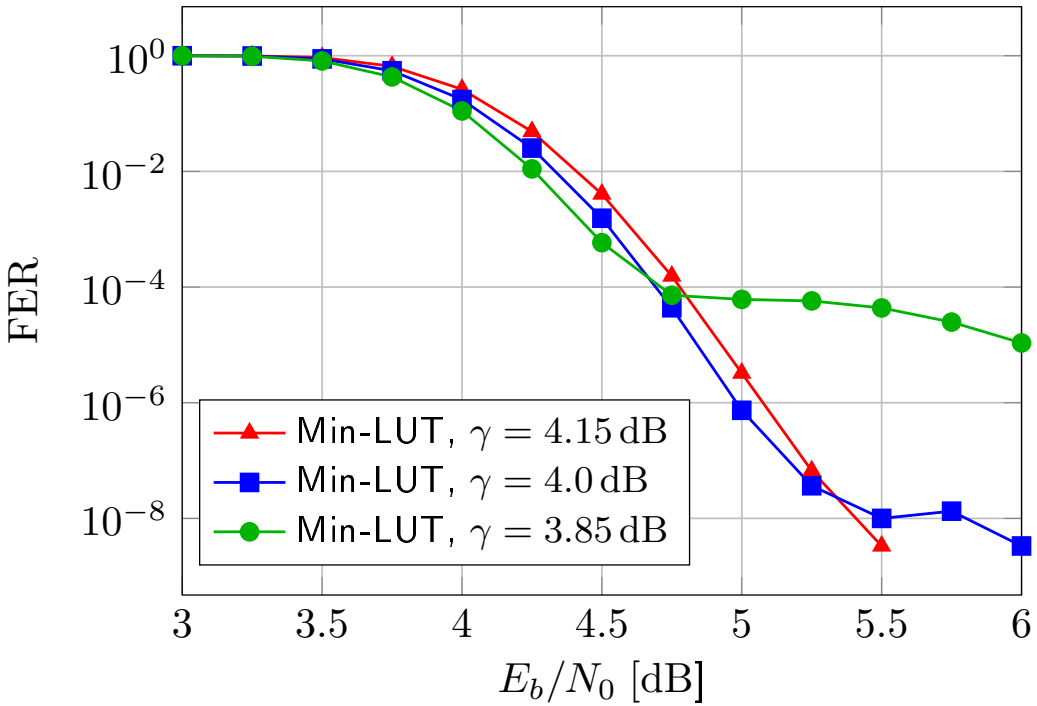

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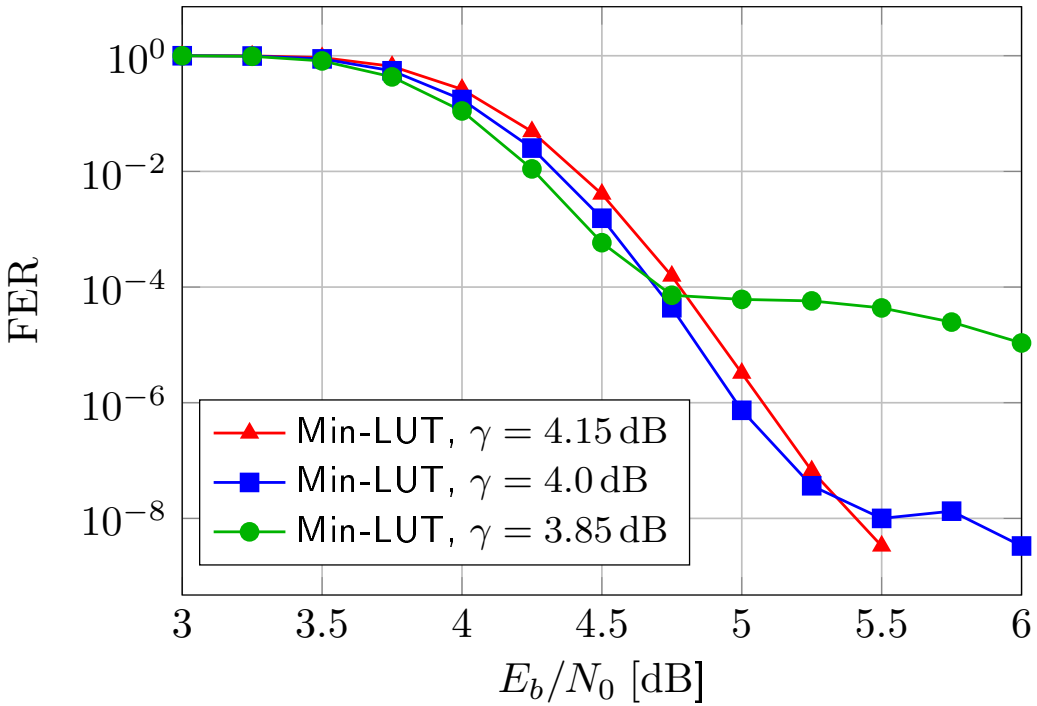

- **Lower design SNR** $\rightarrow$ better **waterfall** region performance.
- **Higher design SNR** $\rightarrow$ better **error floor** region performance.

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Straightforward LUT design:

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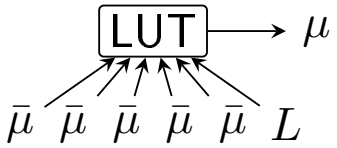

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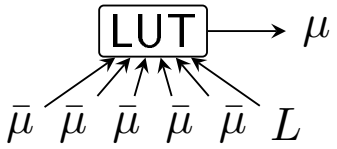

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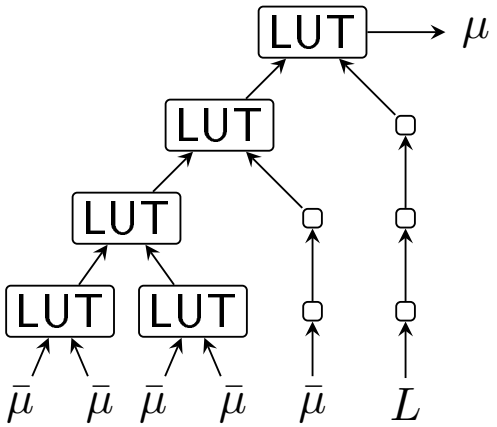

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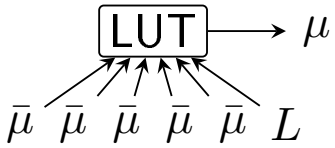

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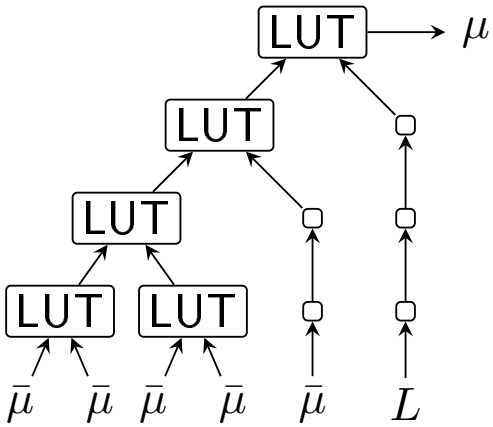

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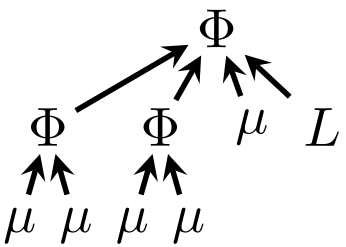
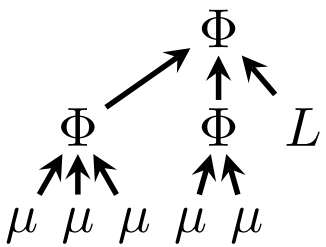
T_1: $\lambda = 10$



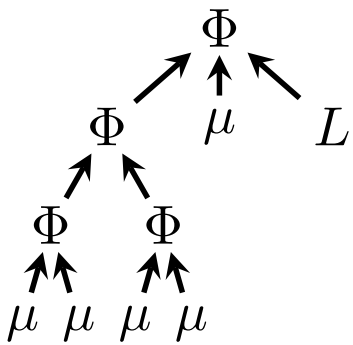
$\sigma_{\text{th}} = 0.5330$

T_2: $\lambda = 11$



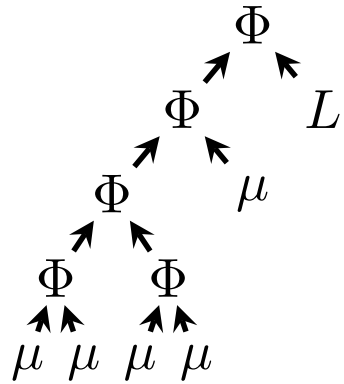
$\sigma_{\text{th}} = 0.5328$

T_3: $\lambda = 14$



$\sigma_{\text{th}} = 0.5313$

T_4: $\lambda = 19$



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Practical Considerations: LUT Tree Structure

- Which trees are preferable?
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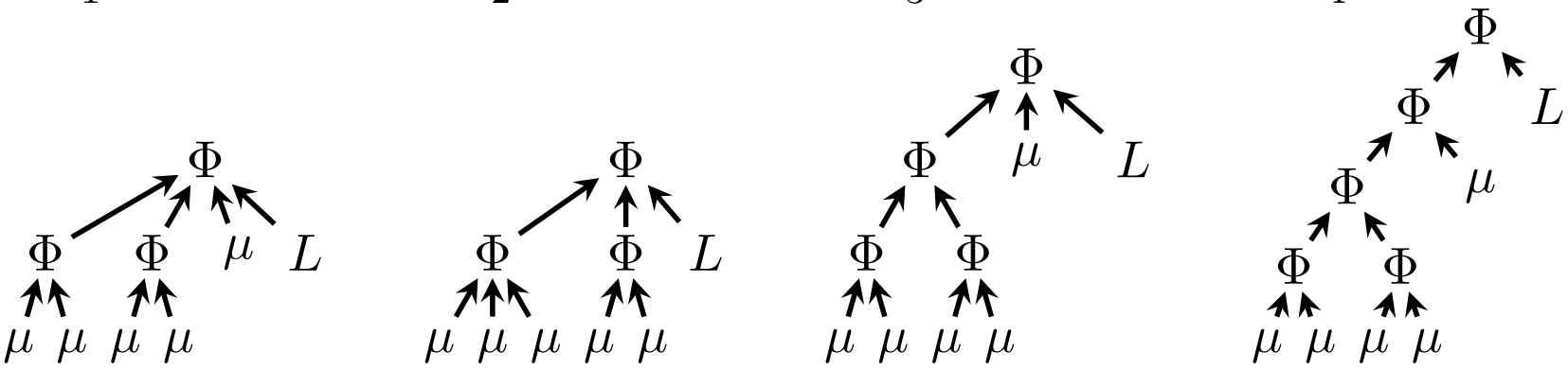

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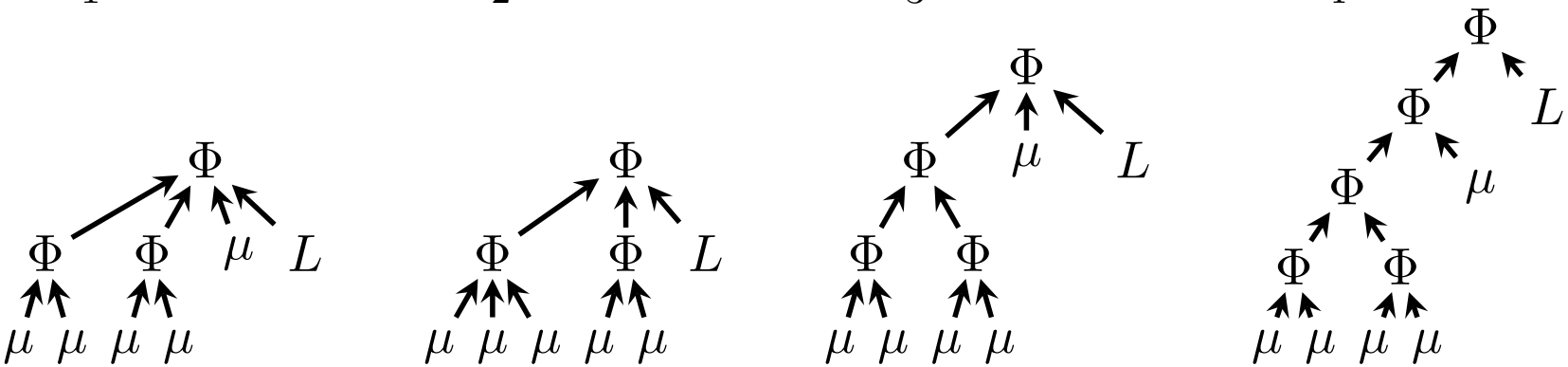

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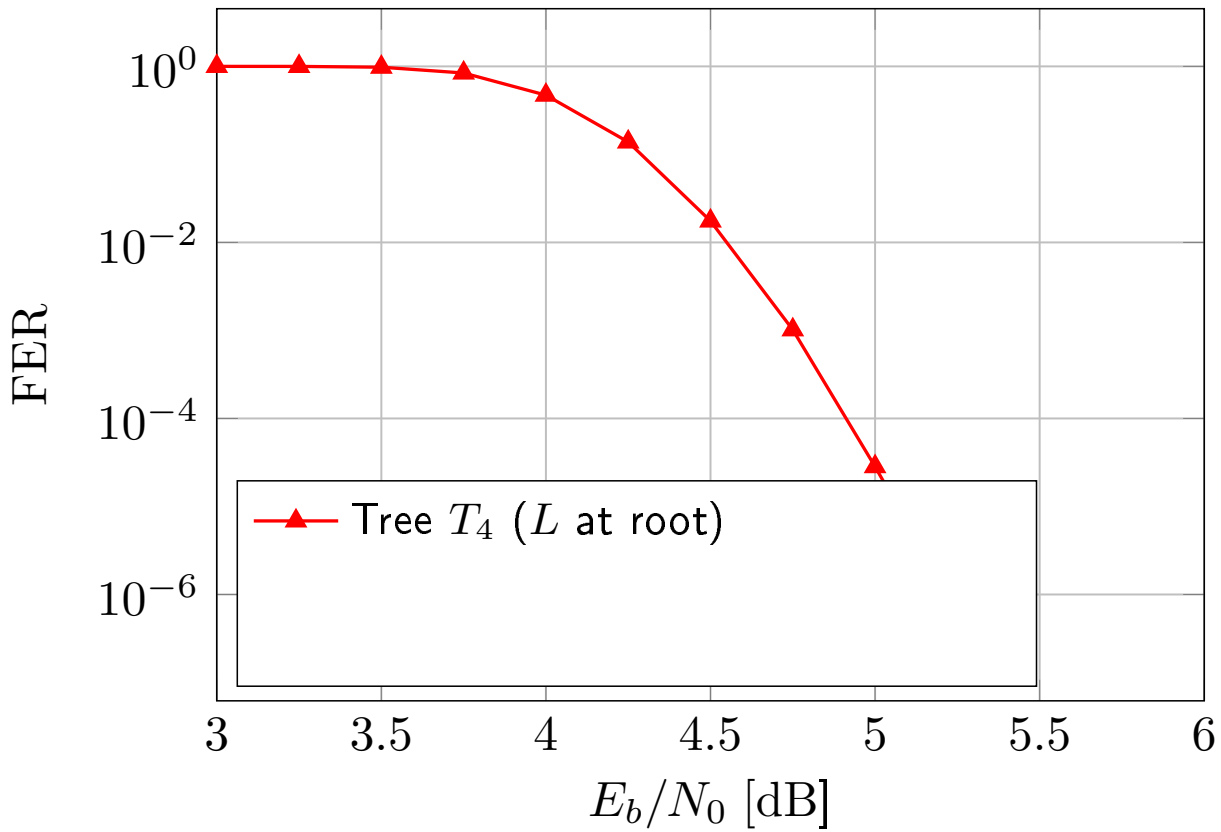
- $T_1 \geq_{\mathcal{T}} T_3 \geq_{\mathcal{T}} T_4$, but, e.g., T_2 and T_1 can not be compared with $\geq_{\mathcal{T}}$.
- Heuristic metric agrees well with density evolution results.

Practical Considerations: Channel LLR Position on LUT Tree

- **Good solution:** L adjacent to the root of the tree.



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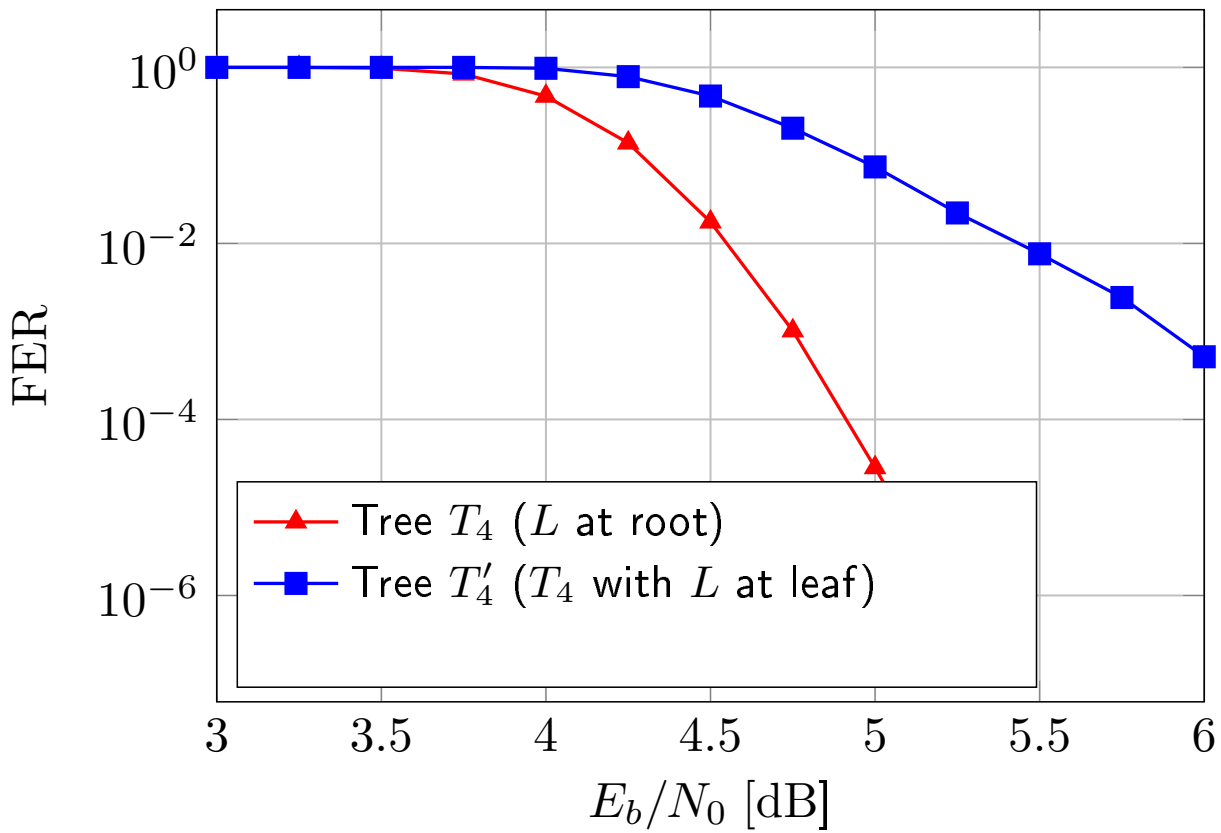

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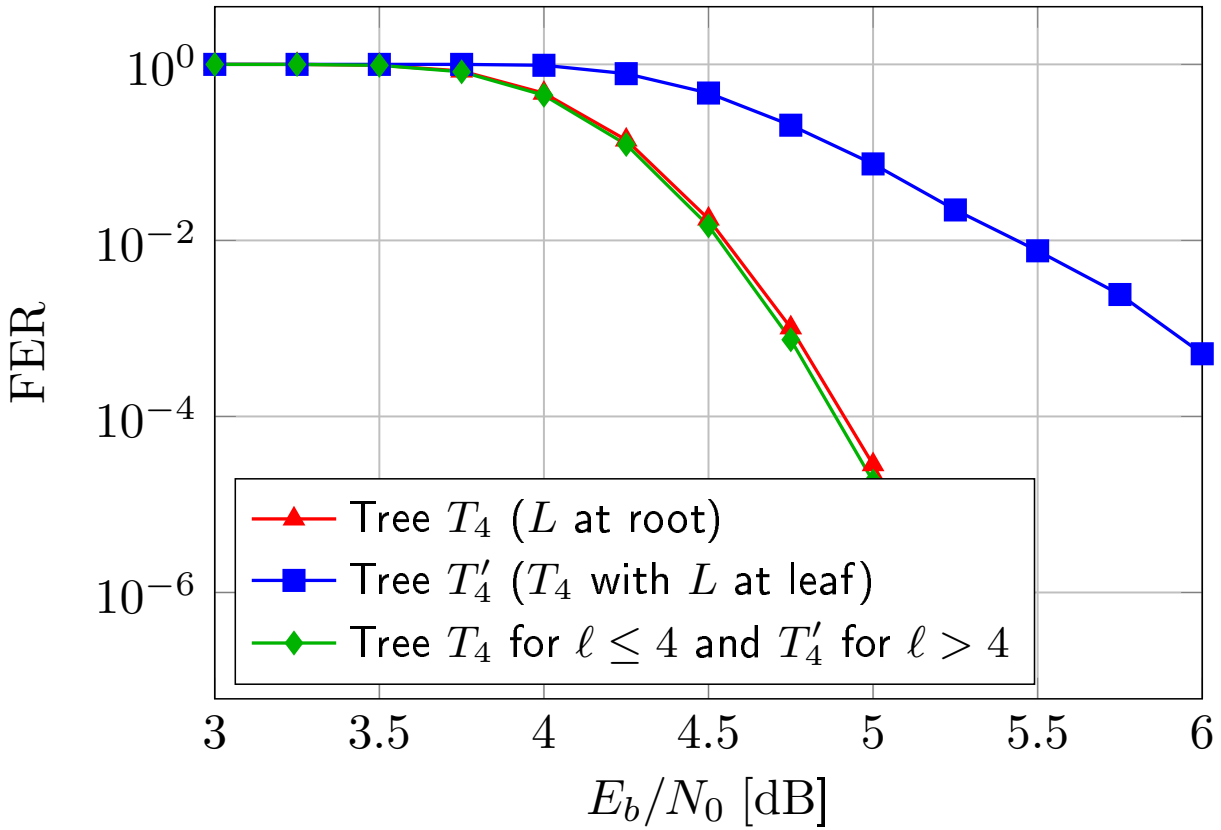
- **Ideal solution:** L close to root for first iterations, farther from root as it becomes more irrelevant.



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Check nodes are ideally also be designed using LUTs.

Unfortunately, CNs can have a large degree (number of inputs) $\rightarrow$ Even tree-structured LUTs become too large/complex.

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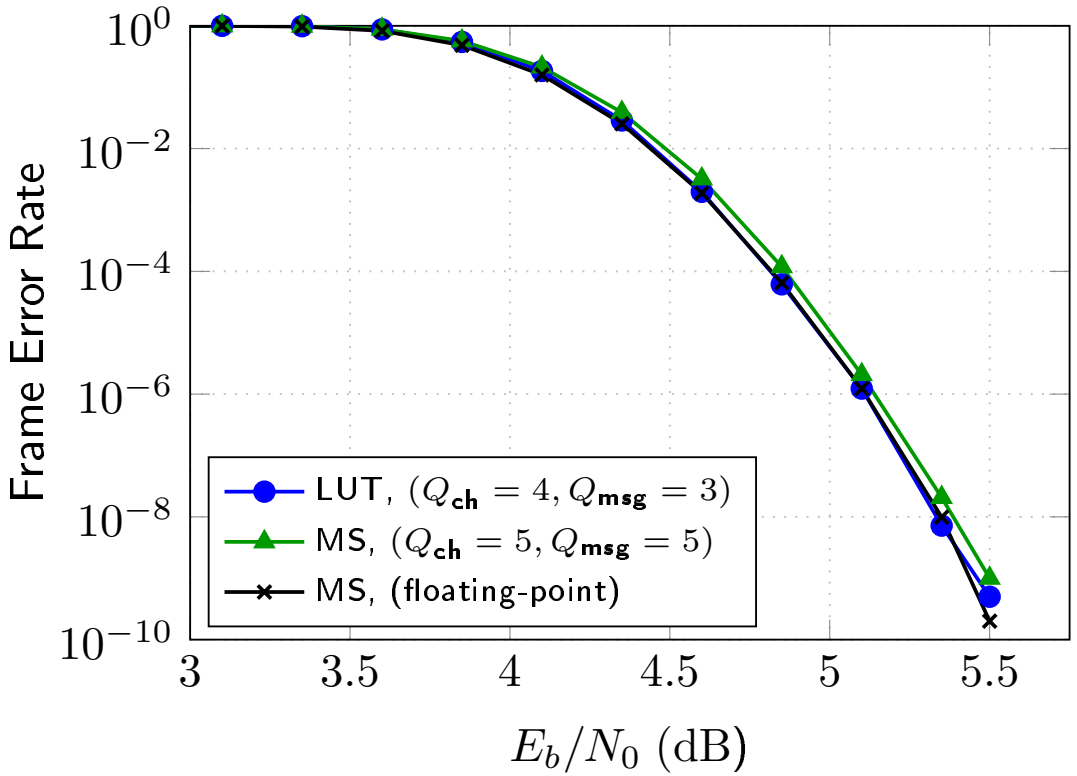
"Min-LUT" Decoder

Entire decoder can be implemented based on **message labels** and CN uses **standard min-sum rule**.

Quantized Message Passing: Quantization

FER performance comparison to Min-Sum decoder with message quantization:



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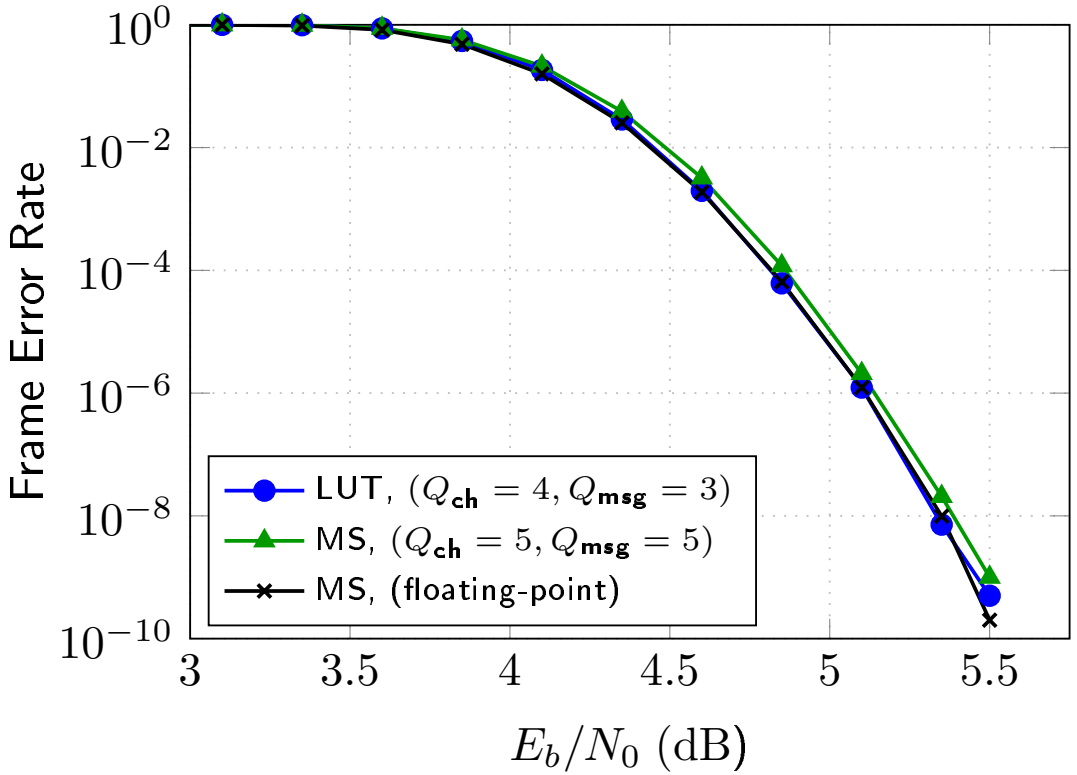

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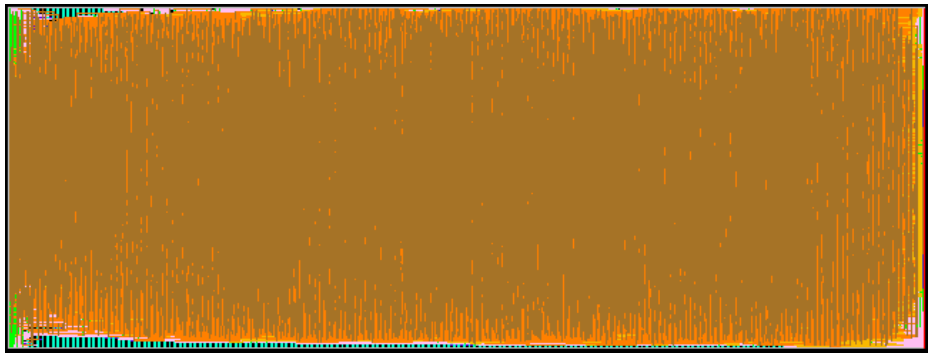
Quantized Message Passing provides **better performance** than regular Min-Sum **with** 40% **fewer message quantization bits**.

Unrolled Quantized Message Passing: Results

Quantization of messages with $Q_{msg} = 3$ bit

- Automatic P&R is finally feasible with **65.9% layout density**



Layout in 28 nm FD-SOI technology

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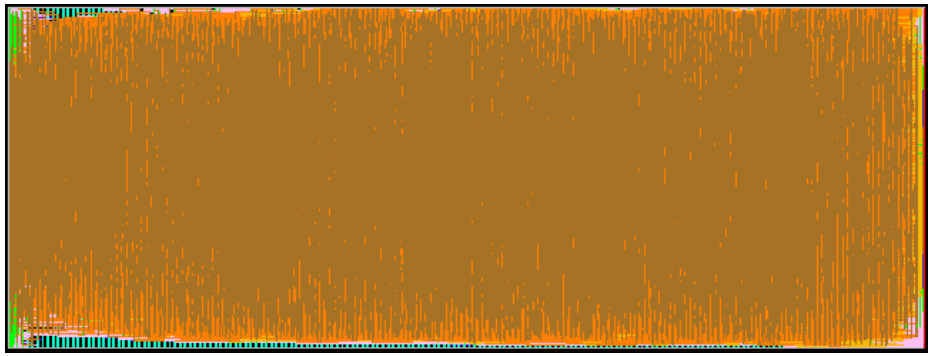

Layout in 28 nm FD-SOI technology

	Unrolled Min-Sum	Unrolled LUT
Msg. Quantization	5 bit	3 bit
Components area (CN/VN) Delay (logic/routing)	3607 μm^2 / 755 μm^2 2.38 ns / 5×1.51 ns	1510 μm^2 / 646 μm^2 1.42 ns / 3×1.16 ns
Core area Throughput	23.3 mm^2 271 Gbps	**16.2 mm^2** **588 Gbps**
Energy efficiency Area efficiency	45.2 pJ/bit 11.6 Gpbs/mm^2	22.7 pJ/bit 36.3 Gpbs/mm^2

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- Further algorithm improvements needed to keep complexity under control
- Need more collaboration between algorithm and architecture design
- Wordlength reduction is one of the most promising objectives

More Information & Code Online

https://www.nt.tuwien.ac.at/UNFOLD