Multicore Architecture and Programming Model Co-Optimization (MAPCO)

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Challenges & Trends in Multicore Processors

Future: Integration of hundreds of cores
Problem: Efficient utilization by applications
Approach: *Joint* optimization of hardware architecture and programming models

Tiled architectures:

- NoC-based, simple RISC cores, distributed memory layout
- Examples: Intel's SCC, Tilera Tile Gx

Problems:

- Threading support
- Efficient communication and synchronization

MAPCO Optimization Approaches

Hardware accelerators to offload cores from overhead of:

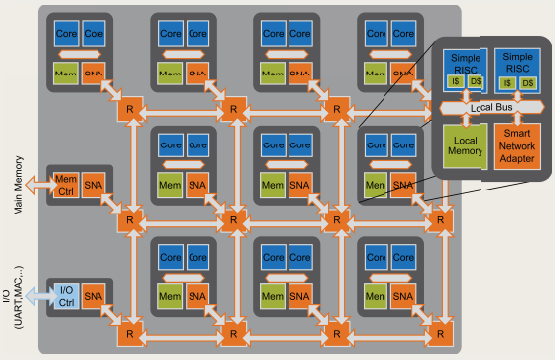
- **Transparent Collective Operations:** reduce overhead of communication and synchronization of threads (presented here)
- **Inter-tile Threading:** Propose a fork-join thread model, explicit communication, HW support for thread handling (presented here)
- **Virtual Hierarchy Network-on-Chip:** Adapting NoC to virtually support application-specific communication patterns

MAPCO Reference Architecture

Generic tiled architecture of:

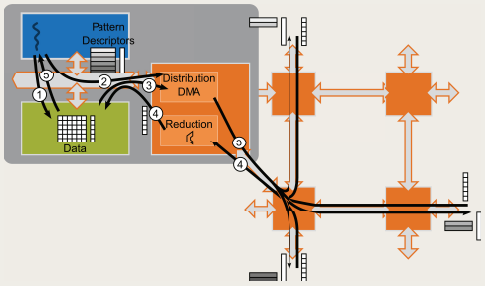
- **Compute Tiles:** 2-8 simple RISC cores, shared memory for message buffers, operating system and thread data
- **Main Memory Tiles:** Distributed memory (DDR, Flash)
- **I/O Tiles:** Ethernet, UART, video I/O, user interface etc.

connected by a NoC: adapter with smart hardware enablement



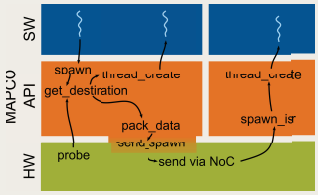
Transparent Collective Operations

- **Smart Network Adapter** (SNA) supports communication
  - Intelligent DMA functionality for data distribution, based on algorithm pattern descriptors (1-3)
  - Transparent gathering and reduction with weakly programmable unit, apply arithmetic and logic operations on incoming data (4,5)

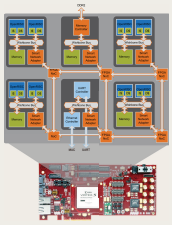


Inter-Tile Threading

- Threading among tiles: fork-join-thread model, transfer context
- Smart Network Adapter handles thread descriptor transfer
- Supported by system and communication load information



Methodology & Outlook



- **Evaluation** methodology:
  - Abstract non-functional simulation
  - Cycle accurate simulation
- Concept **prototyping**:
  - OpenRISC processor (MP extensions)
  - FPGANoC, DDR2 memory, Flash, UART
  - Codezero microkernel, Multicore Association message passing API
- **Status & Outlook**
  - Evaluation and exploration of ideas in high level abstract simulation
  - Accurate performance evaluation for real world algorithms
  - Build basic prototyping platform

More Information: http://www.lis.ei.tum.de
http://www.in.tum.de/?id=mapco

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MAC – Munich Centre of Advanced Computing