Associate Professorship of Embedded Systems and Internet of Things
Department of Electrical and Computer Engineering
Technical University of Munich

FPGA based translation mechanism for TSN

Description of Master's Thesis

November 20, 2022

Title: "FPGA based translation mechanism for TSN"
Supervisor: Rubi Debnath

Context

Time-sensitive network (TSN) enables deterministic transmission on standard Ethernet.
In this topic, the student will implement a new translation mechanism of TSN using VHDL and FPGA. To conclude, the testing will be done in a hardware setup to verify the application.

Requirements

- **Very good VHDL, Verilog, C++ programming skills.**
- **Should be motivated to work in research topics.**
- **Knowledge of communications and networks.**
- **Interest or willing to learn about TSN and 5G.**
- Independent and able to work with minimal supervision.

Contact

If you are interested in this topic, please send your full application (CV, current transcript of records, research interests, possible start dates) to Rubi Debnath (rubi.debnath@tum.de).