Research-Teaching Exchange Excursion from TUM to NIT-Jalandhar

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This is a proposal for a 10 days of study exchange excursion to the National Institute of Technology at Jalandhar, India (NITJ) of a team of four students from the Technische Universität München (TUM), two PhD students and two Masters students. This excursion will be organized on the behalf of Lehrstuhl für Entwurfsautomatiesierung, which comes under the Department of Electrical and Computer Engineering at the TUM. Lehrstuhl für Entwurfsautomatisierung (EDA) is a chair at TUM held by Prof. Dr. Ulf Schlichtmann. The objectives of this excursion are to get an exposure to student activities at the departments of Electronics and Computer Engineering at the NITJ, teaching & research projects, possibilities for improving students-exchange among the participating universities, and gain local cultural experiences. As an effort to extend our teaching/research efforts to reach other talented international researchers & students, we are proposing to organize a three-days of workshop on Xilinx ZedBoard FPGA for the research scholars (masters and PhD) at NITJ. The workshop is an outcome of our previous years of ESL research and the trends we have observed toward the high-performance application-specific computing using FPGAs. The main idea behind organizing this workshop is to introduce the current teachings and on-going research on the embedded-system-level topics at EDA-TUM to the participating researchers and the faculty members. One day of this excursion will be dedicated for the talks from the NITJ research scholars, and a day for exchanging knowledge on teaching & research projects at the participating universities. The remaining days will be spend on traveling, visiting local touristic landmarks and other cultural activities.
This excursion shall align with our institutes effort to invite international researchers/students for internships to our institute for research projects. It will be a good opportunity for the visiting TUM students to learn about the educational and research culture in Indian universities, and network with the local students and academic communities. The close interactions with the local students & faculty members would help learn the working & social habits, which can be a worthwhile personal lesson. Further, this engagement can open-up possibilities for students exchange and future collaborations in teaching or research projects. Participants from TUM,

- *Munish Jassi, Andreas Herrmann, PhD candidates at EDA, TUM*
- *Jian Lyu, Nicolai Oswald, M.Sc. student, TUM*

Schedule for the NITJ-TUM School

15.Sept, THUS, Day-1	Travel from Munich to Amritsar, to Jalandhar. 12:00 - Arrival at the NIT Guest-house.
16.Sept FRI, Day-2	08:30-09:30 - Breakfast 09:30-10:00 - Introduction and Inaugural from NITJ - ECE, CS, ICE departments. 10:00-10:45 - Introduction of TUM and TUM-Team. (Munish Jassi) 10:45-11:15 - University Studies in Germany (Andreas Herrmann) 11:15-11:30 - Applied-Science Studies, Hochschule (Nicolai Oswald) 11:30-11:45 - Internationalization at the University-Level Studies (Jian Lyu) 11:45-13:15 - Visits to NITJ labs, Emerging Tech., VHDL, Bio. Tech., Sig. Processing. 13:15-14:30 - Lunch Break 14:30-16:30 - **Preparations for the workshop** **Evening Social Events:** City tour of Jalandhar (18:00-20:00)
17/18. Sept WE, Day-3/4	**Weekend: Social activities**
19.Sept MON, Day-5	07:30-08:30 - Breakfast **Talks from NITJ research scholars (08:30-16:00):** 1. Design consideration of junction less Transistors (S.Intekhab Amin, faculty) 2. Microcontroller digital IP code (Amandeep Singh, PhD) 3. Spintronics (Naveen Kumar, PhD) 4. Junctionless MOSFET (Sarabdeep Kour, PhD) 5. Charge Plasma based TFET (Sunil Anand, PhD) 6. Vision Enhancement through single Image Fog Removal (Imtiyaz Anwar, PhD) 7. Modified carrier select adder (Sarabdeep Singh, PhD) 8. CNTFET (Shashi Bala, PhD) 9. Image Processing (Tulika, faculty) 10. — — (CSE, —) 11. — — (CSE, —) 12:00-13:00 - Lunch Break **Evening Social Events:** Dinner at ”Haveli Restaurant (19:00-22:00)”
20.Sept TUE, Day-6	**MORNING SESSION: Research Activities at the Institute for EDA at TUM** 07:30-08:30 - Breakfast 08:30-09:15 - Graph-Grammar-Based IP-Integration for SW-Defined SoCs (Jassi) 09-15-10:00 - Aging-aware Optimizations for Analog Circuits (Herrmann) 10:00-10:30 - Coffee Break 10:30-11:00 - Cache Coherency and Memory Consistency in Network-on-Chip (Oswald) 11:30-12:00 - Hardware-Acclerated Motion-Detection on the ZedBoard FPGA (Lyu) 12:00-13:00 - Lunch Break **AFTERNOON SESSION: Basics on VHDL programming (Herrmann, Oswald)** 13:00-13:45 - Introduction talk: IDEA Algorithm on an FPGA, Spartan 3E 13:40-14:30 - Talk: VHDL basics - general syntax, structural and behavioral modeling 14:30-15:30 - Write basic modules in VHDL & respective testbenches 15:30-16:30 - Connect all the modules for the IDEA algorithm and simulate it

21.Sept WED, Day-7	**MORNING SESSION: FSM implementation on FPGA (Herrmann, Oswald)** 07:30-08:30 - Breakfast 08:30-09:30 - Talk: Complete flow from simulating until the FPGA programming 09:30-10:15 - Try to implement it on the board =>Fail, design too big 10:15-11:00 - Talk: FSM modeling and differences between simulation and implementation 11:00-12:00 - Improve design and re-implement it on the board 12:00-13:00 - Lunch Break **AFTERNOON SESSION: Part A: Introduction to ZedBoard (Jassi, Lyu)** 13:00-13:45 - Introduction Talk: Introduction to ZedBoard FPGA and ARM CPU 13:45-14:30 - First project on the ZedBoard: Executing 'Hello World' program via UART. 14:30-16:30 - The LED brightness control application on the ZedBoard - Xilinx ISE **Evening Social Events:** Dinner with NITJ participants at the "Prithvi Planet" (19:00-22:00)
22.Sept THU, Day-8	**MORNING SESSION: Part B: SW-Based Video Processing on ZedBoard (Jassi, Lyu)** 07:30-08:30 - Breakfast 08:30-09:15 - Introduction talk: Virtual Prototyping on the ZedBoard 09:30-10:30 - Implement the Video-processing SoC using the provided base implementation 10:30-11:30 - Implement SW project, fetch video, SW application, display processed image 11:30-12:00 - Program FPGA with HW bit-stream (*.bit) and SW ELF (*.elf) 12:00-13:00 - Lunch Break **AFTERNOON SESSION: Part C: HW-Accelerated Video Processing on ZedBoard** 13:00-13:45 - Introduction talk: IP-integration & HW-acceleration for a System-on-Chip 13:45-14:30 - Accelerate of the software video-processing task using the HW-accelerator 14:30-15:30 - Instantiate and integration required IPs to data & control buses 15:30-16:30 - Do performance analysis to evaluate the improvements
23.Sept FRI, Day-9	07:30-08:30 - Breakfast 08:30-12:00 - **Discussions:** Research projects/student-exchange between TUM and NITJ 12:00-13:00 - Lunch Break
24.Sept SAT,Day-10	09:00 - Travel from Jalandhar to Delhi, to Munich

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