Chair of Network Architectures and Services
TUM School of Computation, Information and Technology
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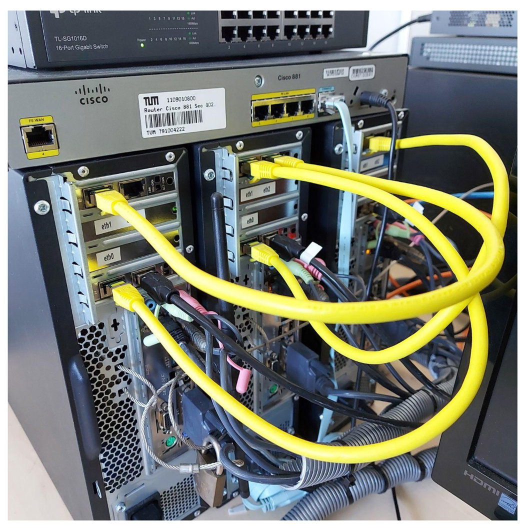
Container and Low Latency Networking

Containing Low Tail-Latencies in Packet Processing Using Lightweight Virtualization

Motivation

Tail-latency Experiments on Real Hardware

- Expensive
- Restrictions on creating arbitrary topologies
- Limited availability
- Can have long delivery times
- Difficult to reproduce



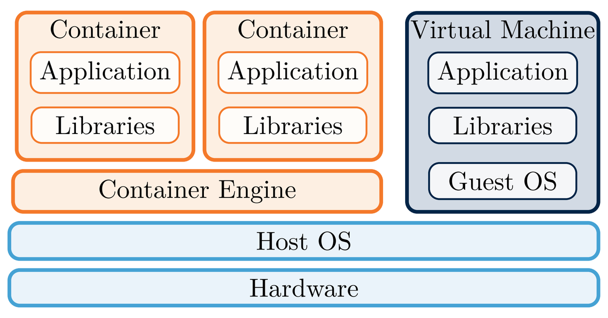
Tail-latency Experiments on Virtual Machines [8]

- Substantial overhead
- Complete Operating System for every machine
- long booting times

Background

Virtualization of systems is possible using:

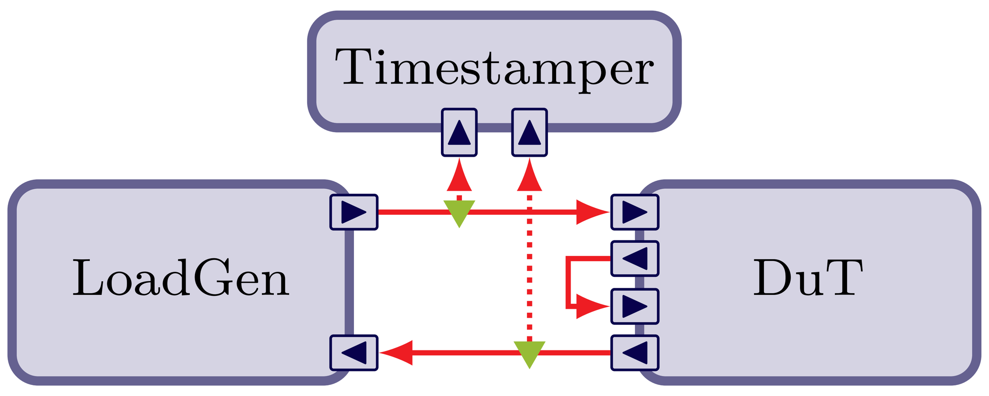
- Full virtualization, e.g., virtual machines (VMs)
- OS-level virtualization, e.g., container



Analyzed raise of latency is according to [2] mostly caused by:

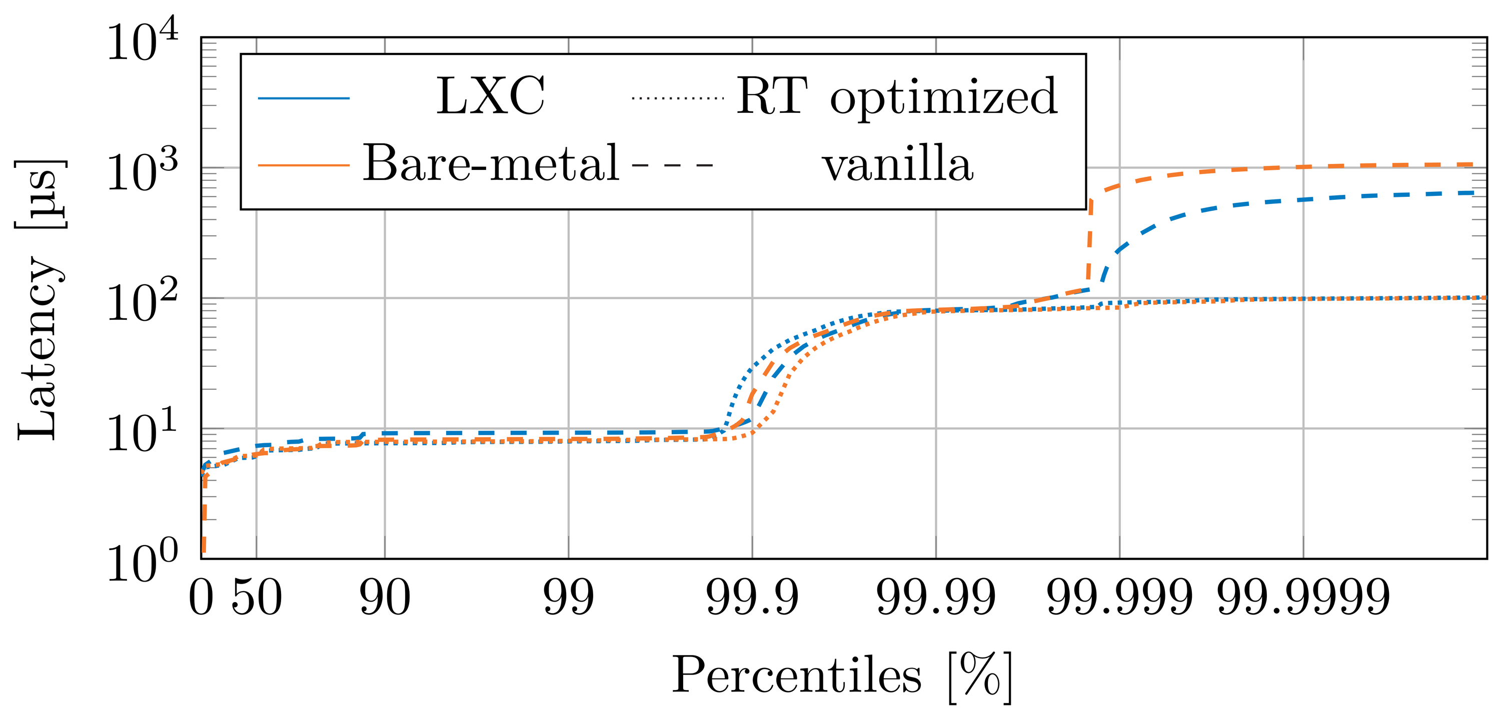
- Interrupts raised on the same core as the virtualization
- Energy-saving mechanism during idle times
- Other applications running on the same cores as the virtualization

Measurement Setup



- Loadgen runs a packet generator (MoonGen [1]) creating UDP packets
- Device under Test (DuT) contains to be analyzed system
- Timestamper records ingress/egress traffic using passive optical traffic access points (TAPs)
  - Hardware-timestamping of entire network traffic (resolution 1.25 ns)
  - Determine worst-case latencies on a per-flow basis

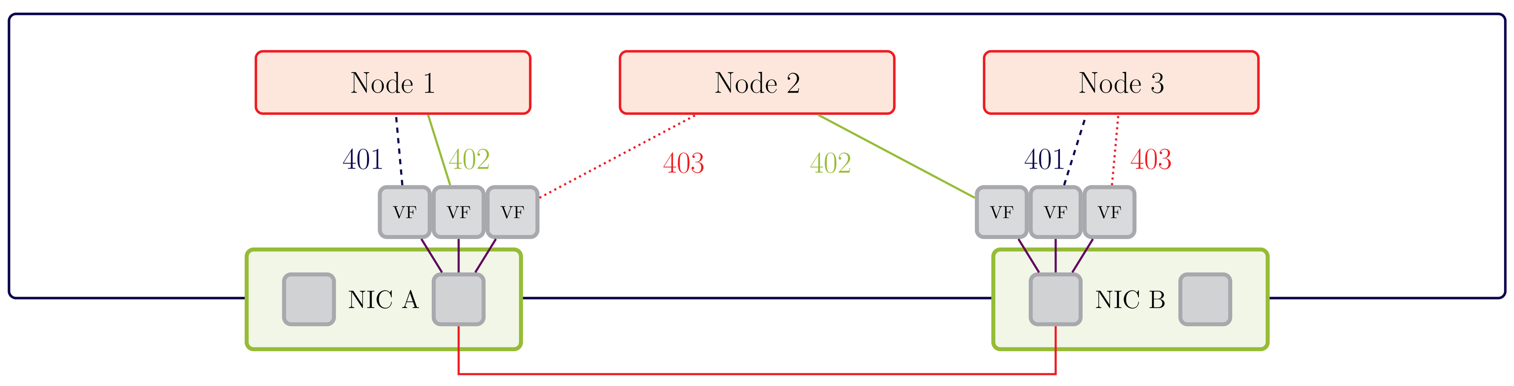
Area A: Tail-latency measurements [6]



Performance of LXC container vs bare-metal using 1 mpackets/s

- Using optimizations such as to:
  - reduce interrupts
  - reduce timer-ticks
  - disable energy-saving-mechanism

Area B: HVNet - Virtualization of topologies [8]



- One VLAN-ID per connection
- Each packet traverses the wire per link once
- Reduce impact using optimization such as core isolation [3]

Area C: Modeling and further analysis

Platform	Opt.	RT	NoHz	Vanilla	Exceedances
VM	✓	✗	✗	✓	1.25
VM	✗	✗	✗	✓	2.58
Container	✓	✓	✗	✗	1.42
Container	✗	✓	✗	✗	7.67
Container	✓	✗	✓	✗	1.25
Container	✗	✗	✓	✗	1.67
Container	✓	✗	✗	✓	2.92
Container	✗	✗	✗	✓	2.29
Kernel Netw.	✓	✓	✗	✗	2.50
Kernel Netw.	✗	✗	✗	✓	22.73

Further, we use our system to:

- QoS-aware routing algorithms in different scenarios [5]
- Compare VM and container on different hardware machines [7]
- model and predict flow-behavior, e.g.,[4].

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[2] S. Gallenmüller, J. Naab, I. Adam, and G. Carle. 5G URLLC: A Case Study on Low-Latency Intrusion Prevention. *IEEE Commun. Mag.*, 58(10):35–41, 2020.
[3] S. Gallenmüller, F. Wiedner, J. Naab, and G. Carle. Ducked Tails: Trimming the Tail Latency of(f) Packet Processing Systems. In P. Chemouil, M. Ulema, S. Clayman, M. Sayit, C. Çetinkaya, and S. Secci, editors, *17th International Conference on Network and Service Management, CNSM 2021, Izmir, Turkey, October 25-29, 2021*, pages 537–543. IEEE, 2021.
[4] M. Helm, F. Wiedner, and G. Carle. Flow-level tail latency estimation and verification based on extreme value theory. In *18th International Conference on Network and Service Management (CNSM) (CNSM 2022)*, Thessaloniki, Greece, Oct. 2022.
[5] F. Wiedner, J. Andre, P. Mendes, and G. Carle. Policy-based routing for Flying Adhoc Networks. In K. R. Chowdhury and W. Jaafar, editors, *DroNet@MobiSys 2022: Proceedings of the Eighth Workshop on Micro Aerial Vehicle Networks, Systems, and Applications, Portland, OR, USA, 1 July 2022*, pages 25–30. ACM, 2022.
[6] F. Wiedner, M. Helm, A. Daichendt, J. Andre, and G. Carle. Containing low tail-latencies in packet processing using lightweight virtualization. In *35th International Teletraffic Congress, ITC 2023, Turin, Italy, October 3-5, 2023*, pages 1–9. IEEE, 2023.
[7] F. Wiedner, M. Helm, A. Daichendt, J. Andre, and G. Carle. Performance evaluation of containers for low-latency packet processing in virtualized network environments. *Perform. Evaluation*, 166:102442, 2024.
[8] F. Wiedner, M. Helm, S. Gallenmüller, and G. Carle. HVNet: Hardware-Assisted Virtual Networking on a Single Physical Host. In *IEEE INFOCOM 2022 - IEEE Conference on Computer Communications Workshops, INFOCOM 2022 - Workshops, New York, NY, USA, May 2-5, 2022*, pages 1–6. IEEE, 2022.

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