Managing Heterogeneous Topologies and Understanding Their Impact on Performance

Doctoral Showcase

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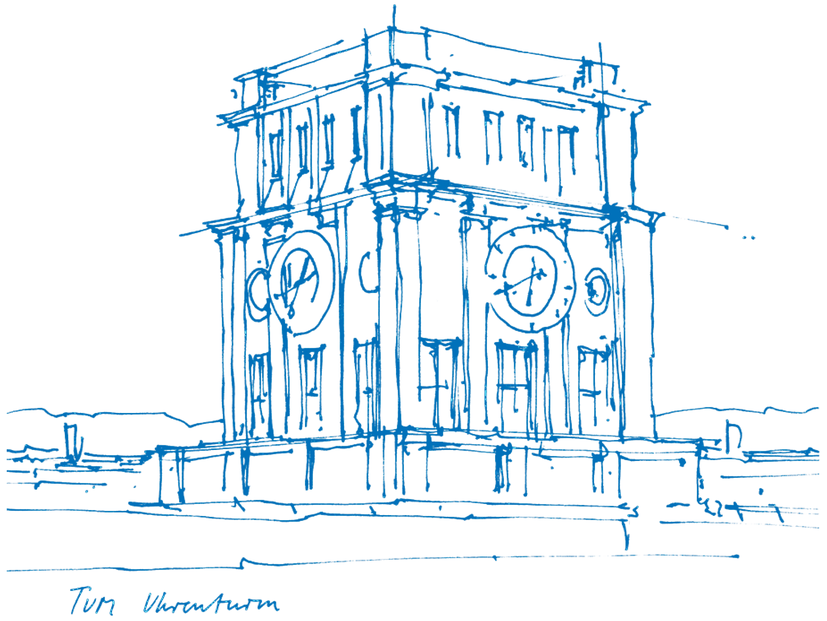

Doctoral Showcase Poster SC'25, 20th November 2025

Motivation

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1 Topologies are increasingly complex

- Heterogeneous
- Dynamic, configurable

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2 Memories play a crucial role

- More parallelism in compute
  - ➡ Higher demand for data
- More complex memory hierarchies
  - ➡ More difficult to understand and tune performance
- More heterogeneous systems, chips, memories
  - ➡ Portability issues

Toolchain Overview

	Topology	GPUs	Memory	Performance Analysis and Modelling	Heterogeneous Chip and Memory Architectures
sys-sage	✅	☑	✅	☑	✅
MT4G	✅	✅	✅	☑	☑
GPUscout	☑	✅	✅	✅	
CXL data transfer modelling	☑		✅	✅	✅
Mitos-MemAxes toolchain	☑		✅	✅	

✅ = core focus ; ☑ = related topic

1. sys-sage

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- Multiple tools (such as hwloc) provide static topological snapshot
- Increased need for dynamic/runtime data (interfaces also exist)
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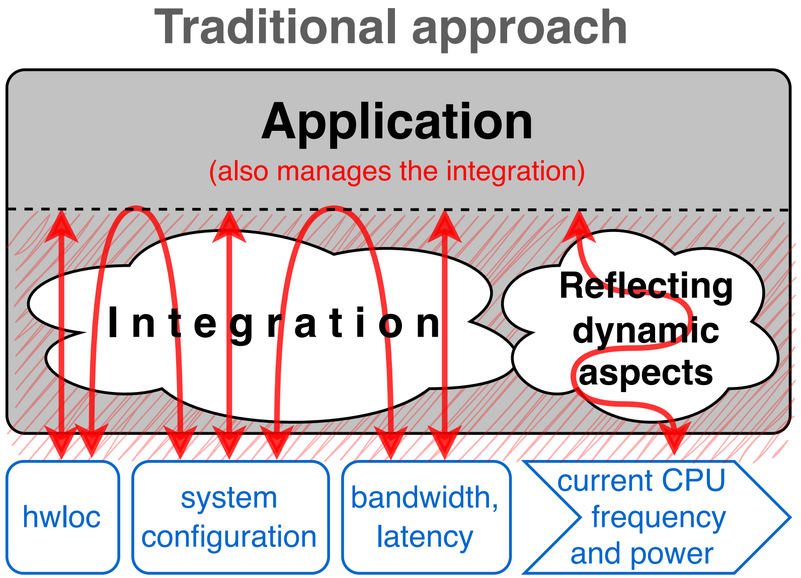

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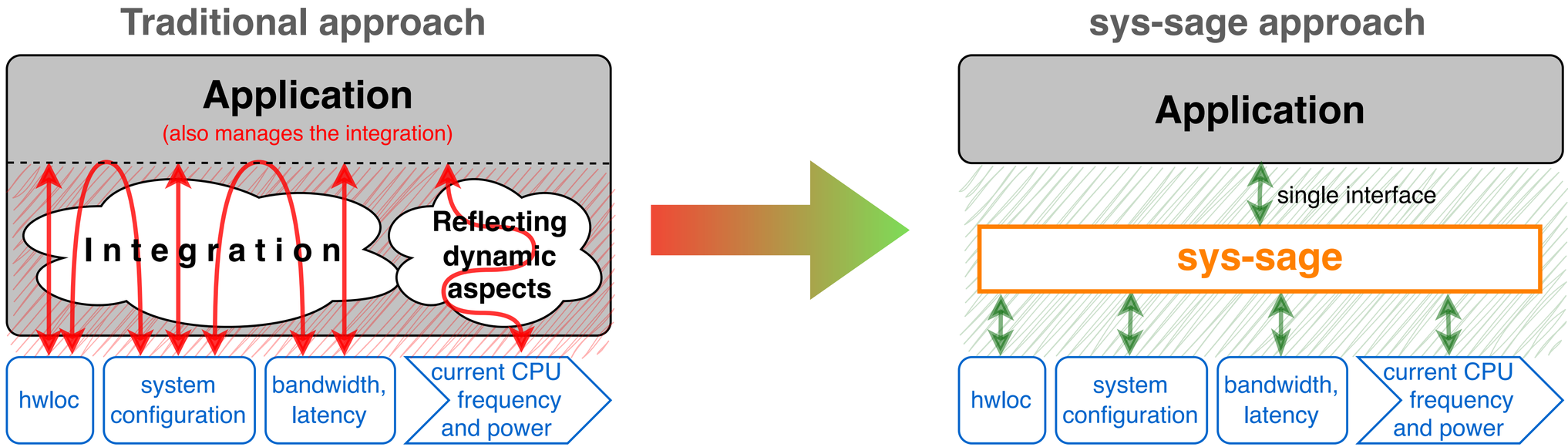

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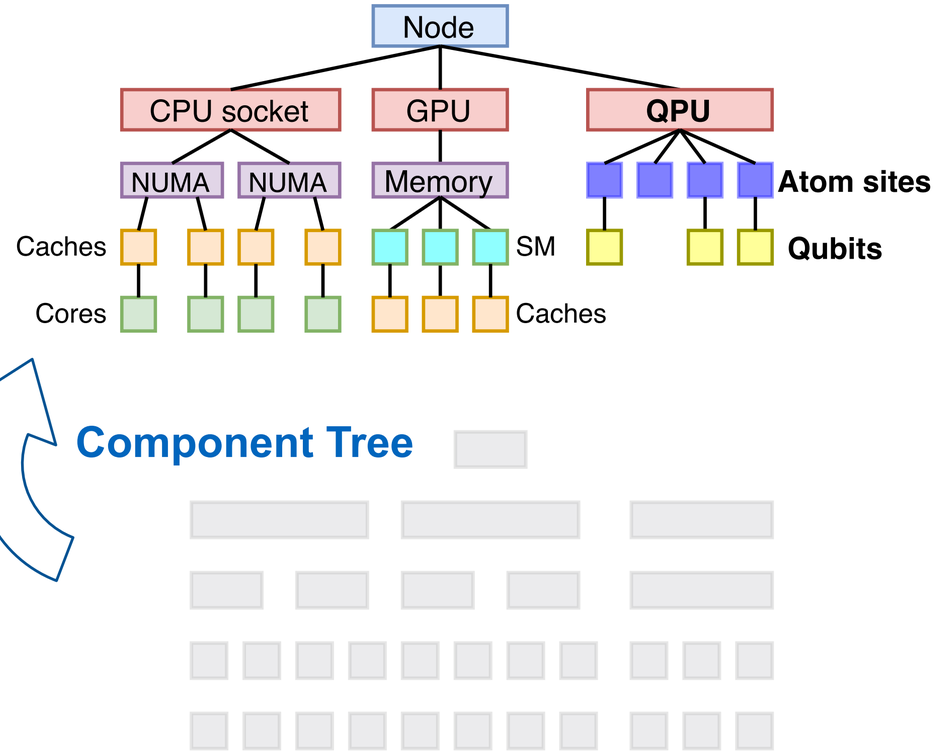
1. Components

- Hierarchical representation (hwloc-like)
- Simple to understand, Mandatory
- Examples: Static CPU/GPU/QPU HW topologies



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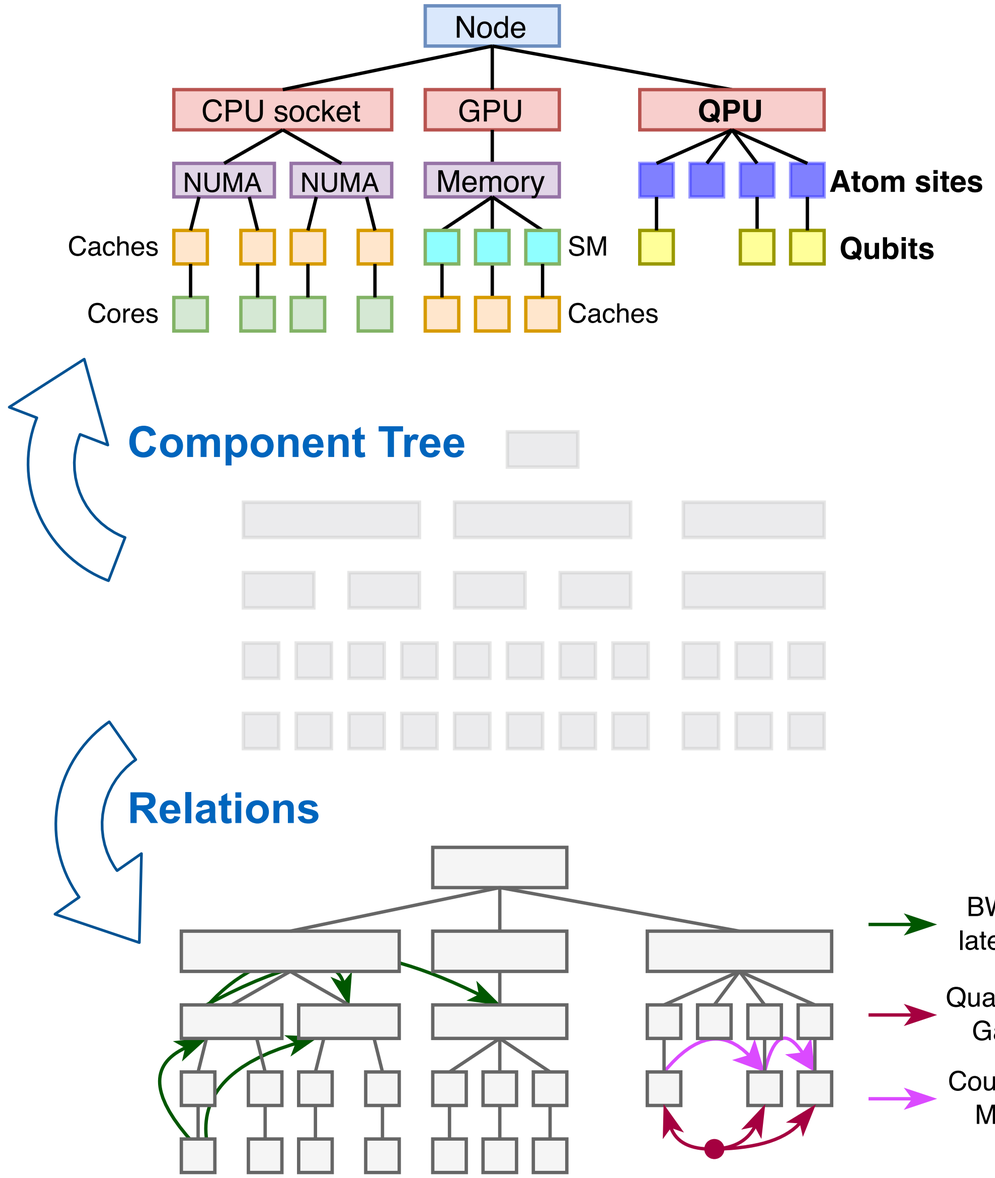
2. Relations

- Any Relation of 1 or more Components
- Orthogonal to the Component Tree
- More dynamic, complex information
- Examples: data exchange rates between components, dynamic settings, HW counter readings



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Quantum Extension

- Quantum Processing Units (QPUs) begin to accompany CPUs and GPUs in HPC systems
- sys-sage was extended to support QPUs alongside CPUs/GPUs
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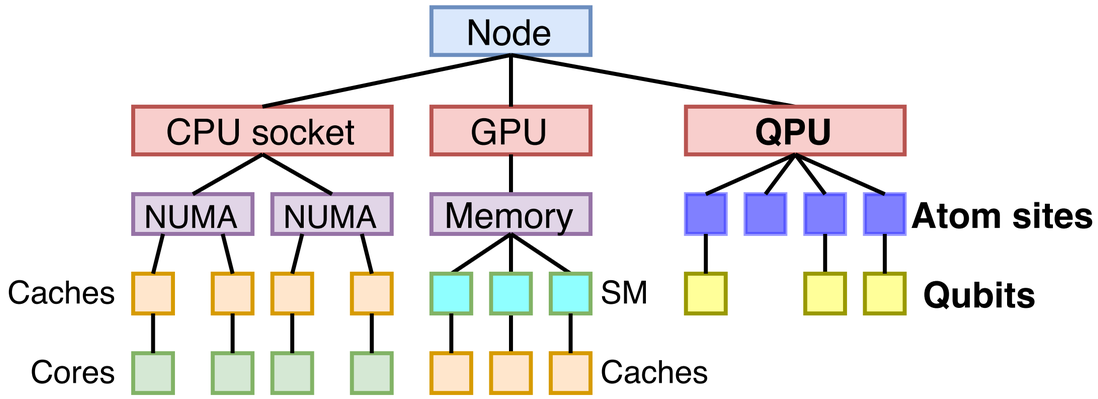

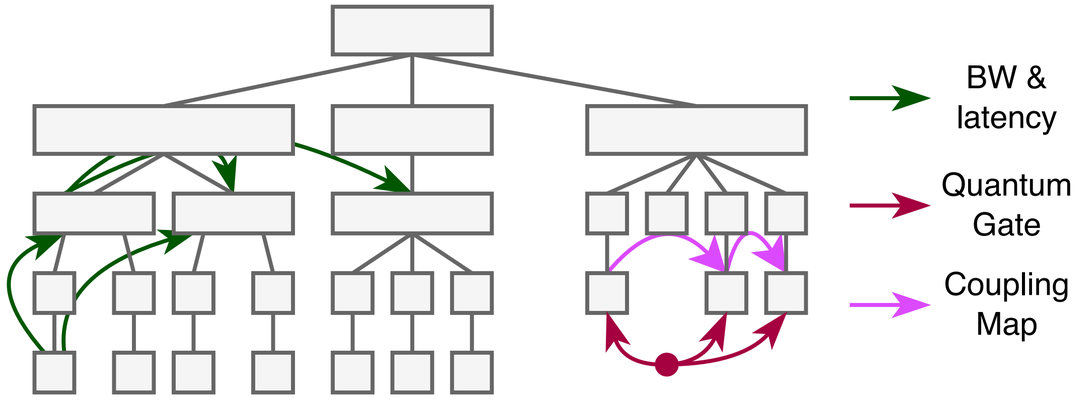

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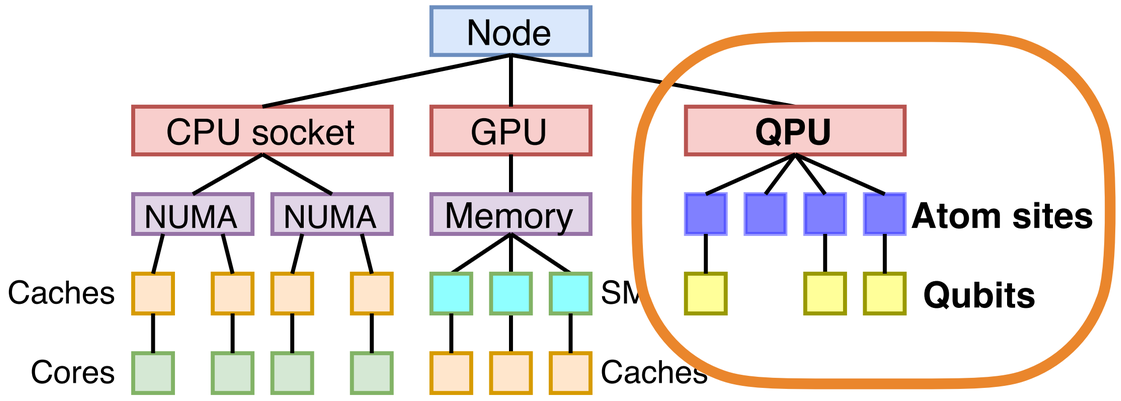

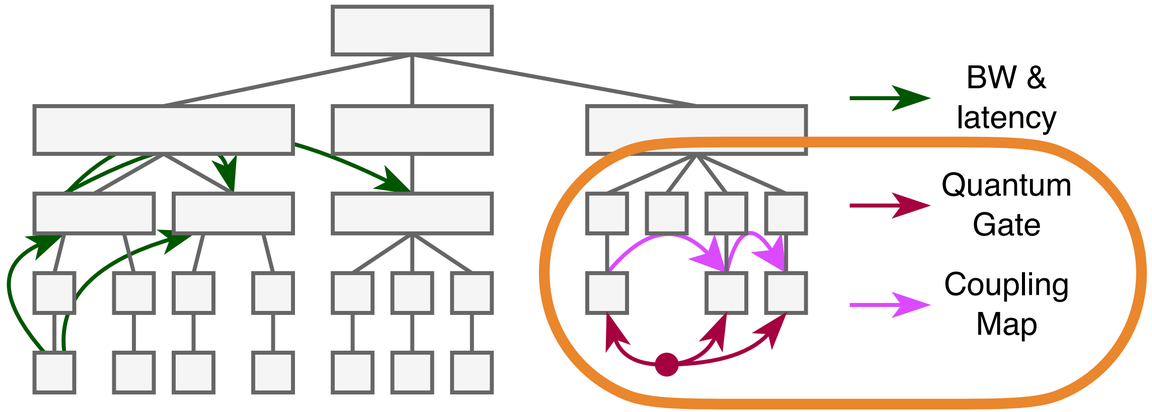

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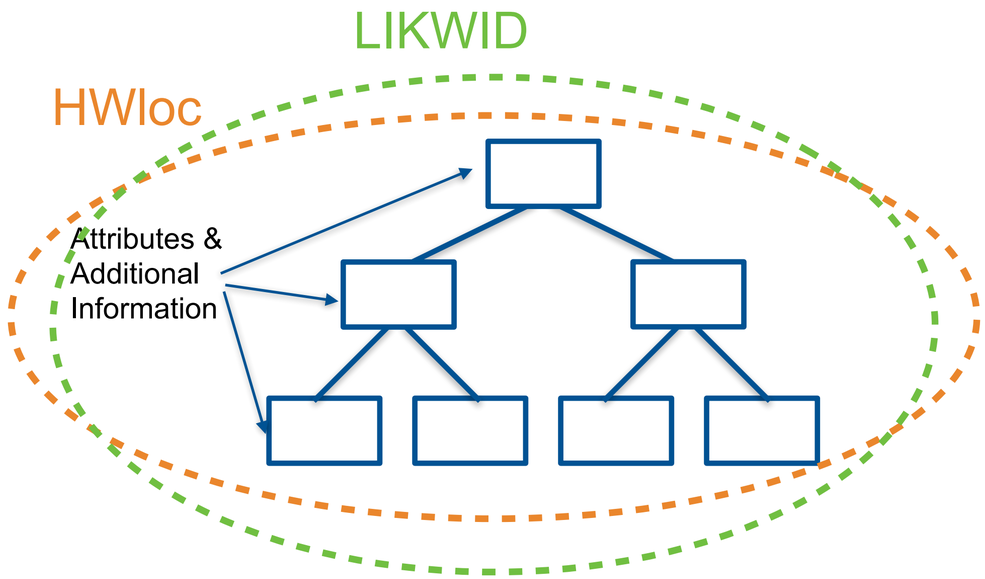
CPUs

Complete, cross-vendor



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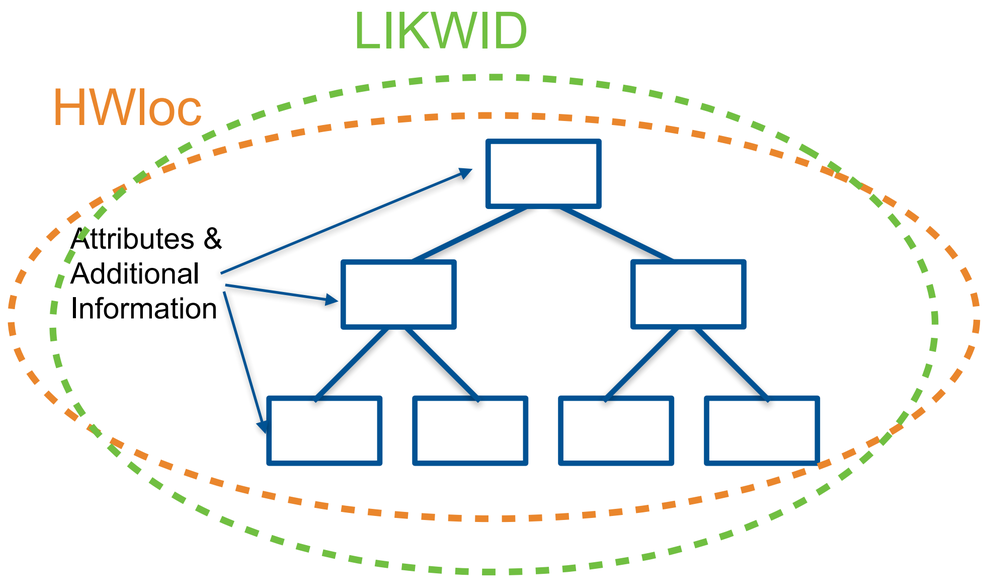
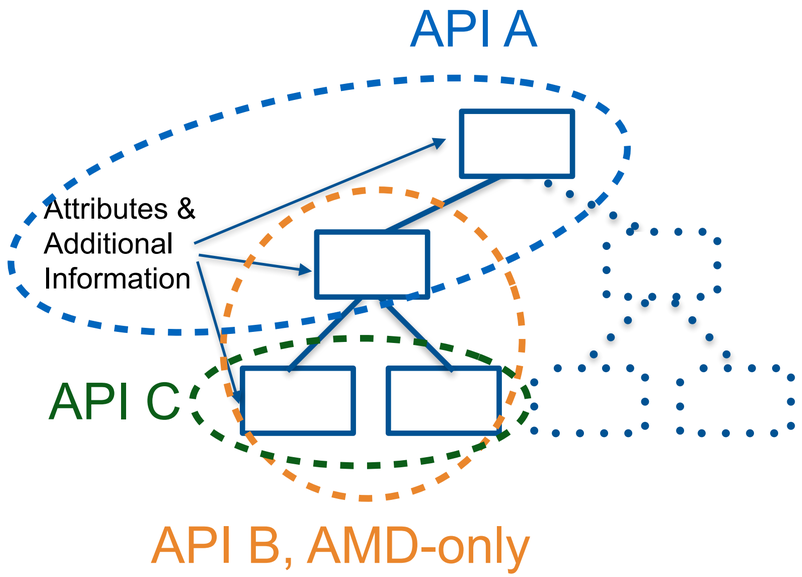


GPUs

Incomplete, scattered, vendor-specific



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Report on GPU building blocks and their attributes and capabilities

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Target Memory Elements

NVIDIA

- L1 cache
- L2 cache
- Texture & Readonly cache
- Constant L1, L1.5 cache
- Shared memory
- Device memory

AMD

- L1 cache
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Queried properties

- Size
- Cache Line Size ($-only)
- Fetch Granularity ($-only)
- Physical Layout
- Load Latency
- Read & Write Bandwidth (L2 cache and above)

\+ Compute Resource Topological Information

2. MT4G — Coverage

✅ = Available via microbenchmark; ☑️ = Available via API; ➡️SOON = Bandwidth only for higher-level elements; ❌ = not available

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Memory Element	Size		LD lat		R&W BW		cache line size		fetch granularity		Amount per SM/GPU		Physical hardware sharing	
Vendor	*NV*	*AMD*	*NV*	*AMD*	*NV*	*AMD*	*NV*	*AMD*	*NV*	*AMD*	*NV*	*AMD*	*NV*	*AMD*
(v) L1 cache	✅	✅	✅	✅	SOON	SOON	✅	✅	✅	✅	✅	✅	✅	
sL1 cache		✅		✅		SOON		✅		✅				✅
L2 cache	☑	☑	✅	✅	✅	✅	✅	☑	✅	✅	✅	☑		
L3 cache		☑		❌		✅		☑		❌		☑		
Texture cache	✅		✅		SOON		✅		✅		✅		✅	
Readonly cache	✅		✅		SOON		✅		✅		✅		✅	
Constant L1 cache	✅		✅		SOON		✅		✅		✅		✅	
Constant L1.5 cache	✅		✅		SOON		❌		✅		❌			
Shared Mem. / LDS	☑	☑	✅	✅	SOON	SOON								
Device Memory	☑	☑	✅	✅	✅	✅								

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3. Collecting performance metrics

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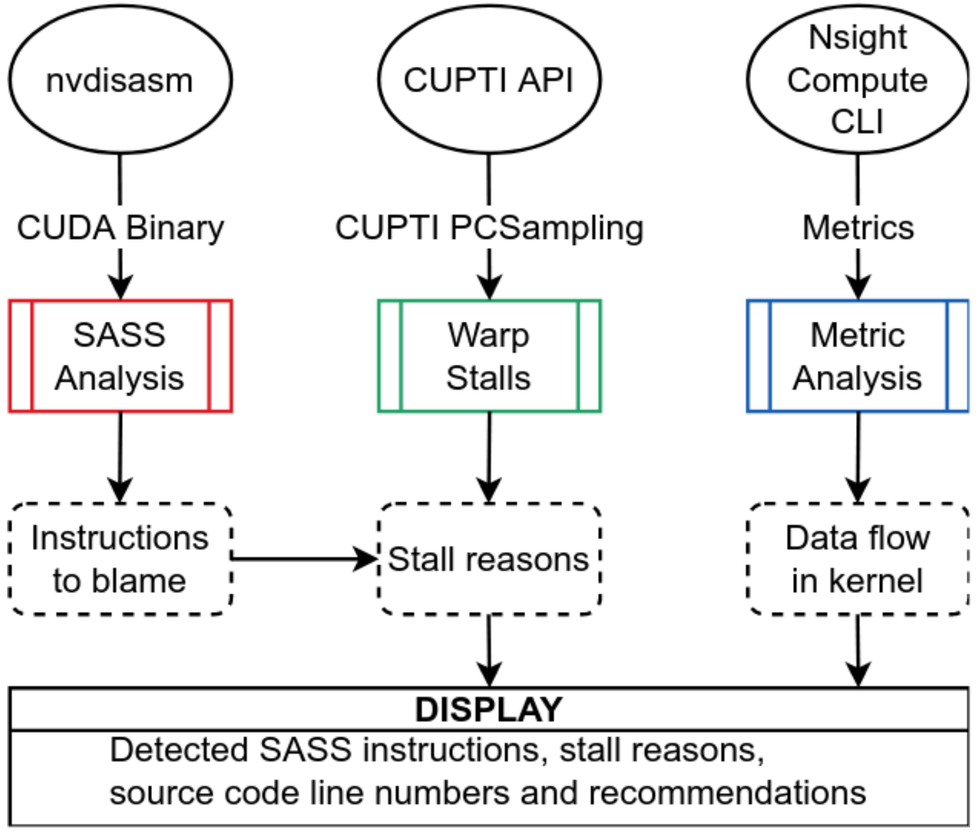

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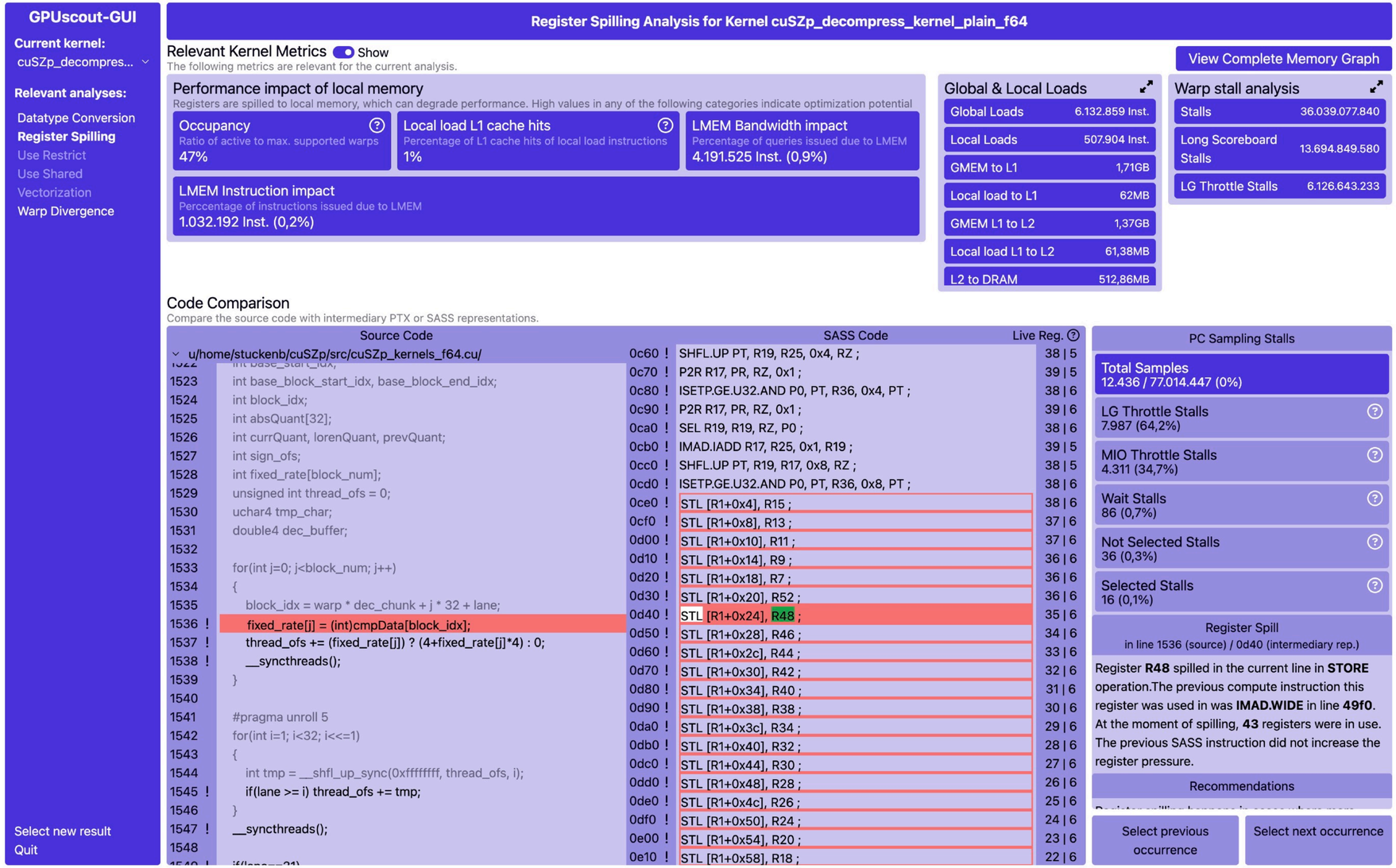

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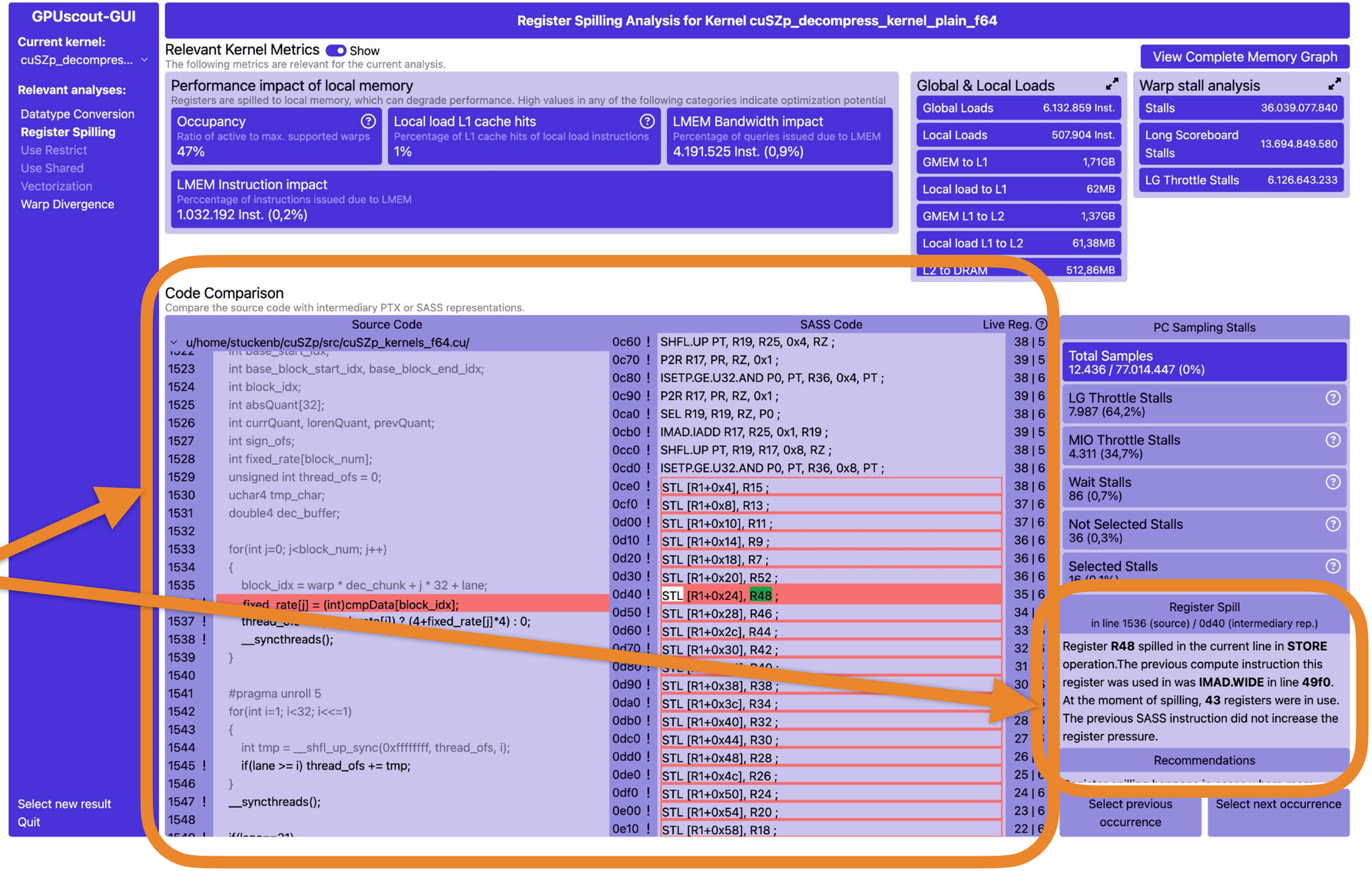

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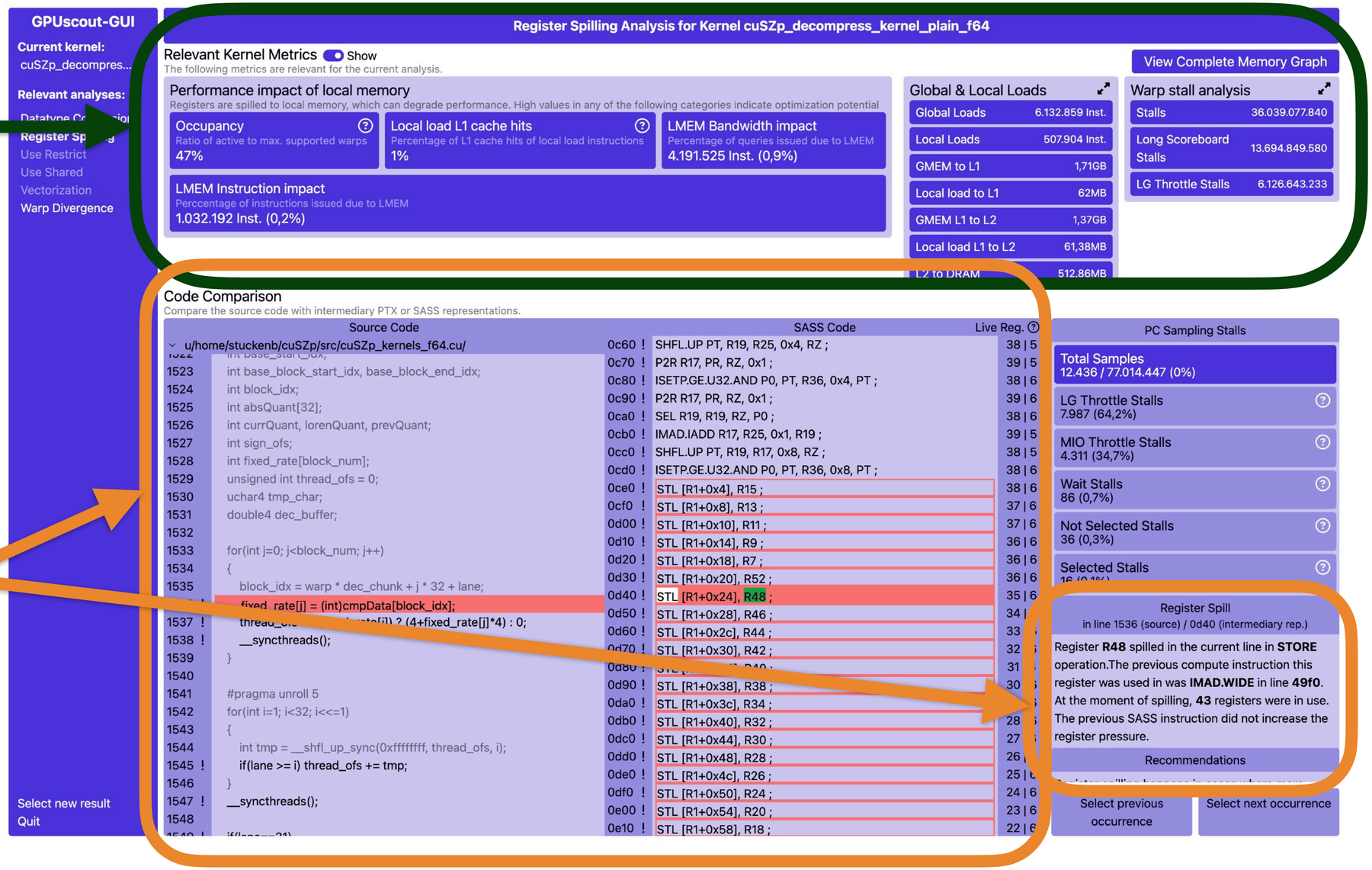
Kernel Metrics

Static Code Analysis



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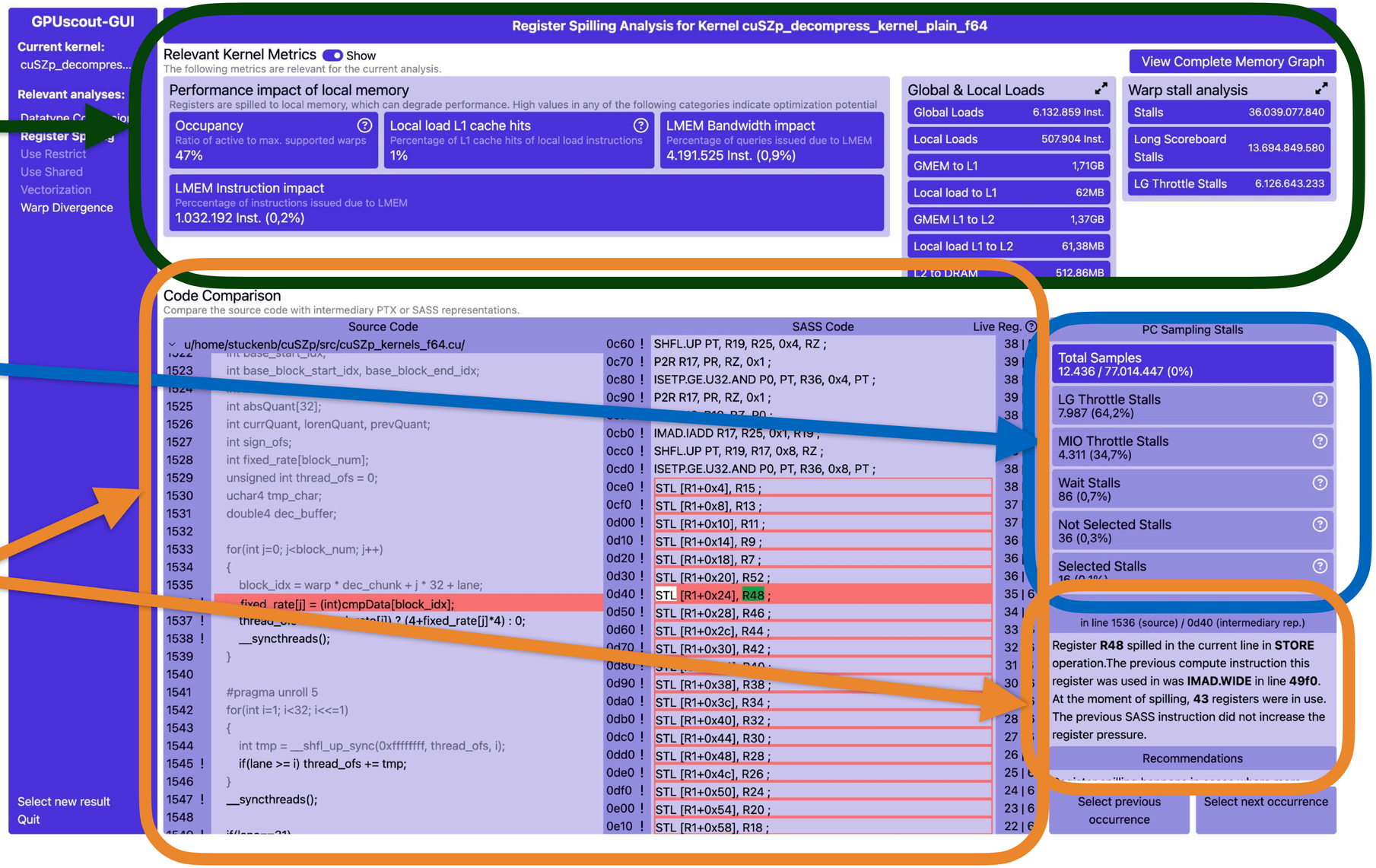

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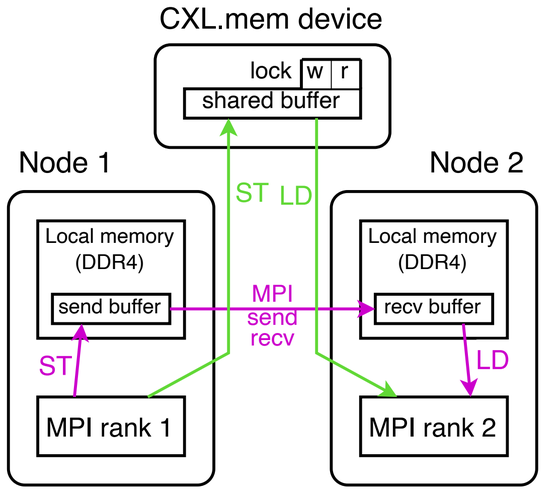

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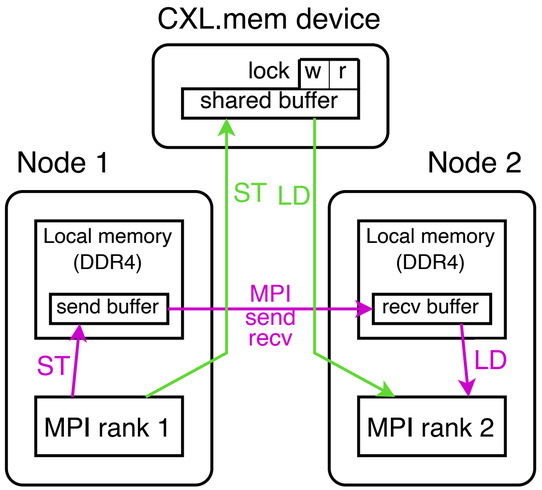
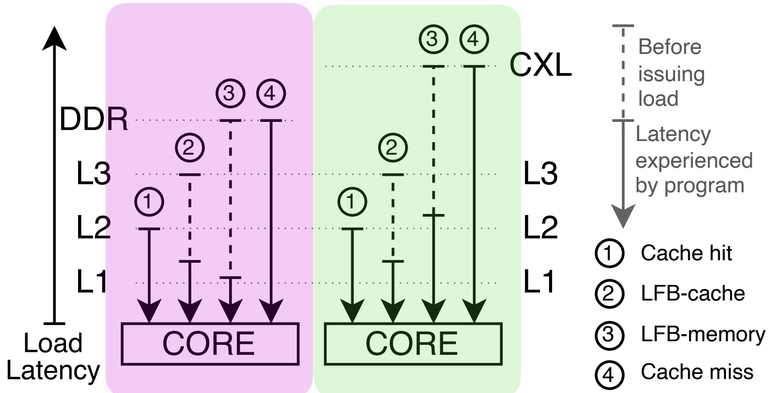


2. Impact on data access patterns



Managing Heterogeneous Topologies and Understanding Their Impact on Performance

Toolchain for understanding system topologies and impact of data transfers on system performance

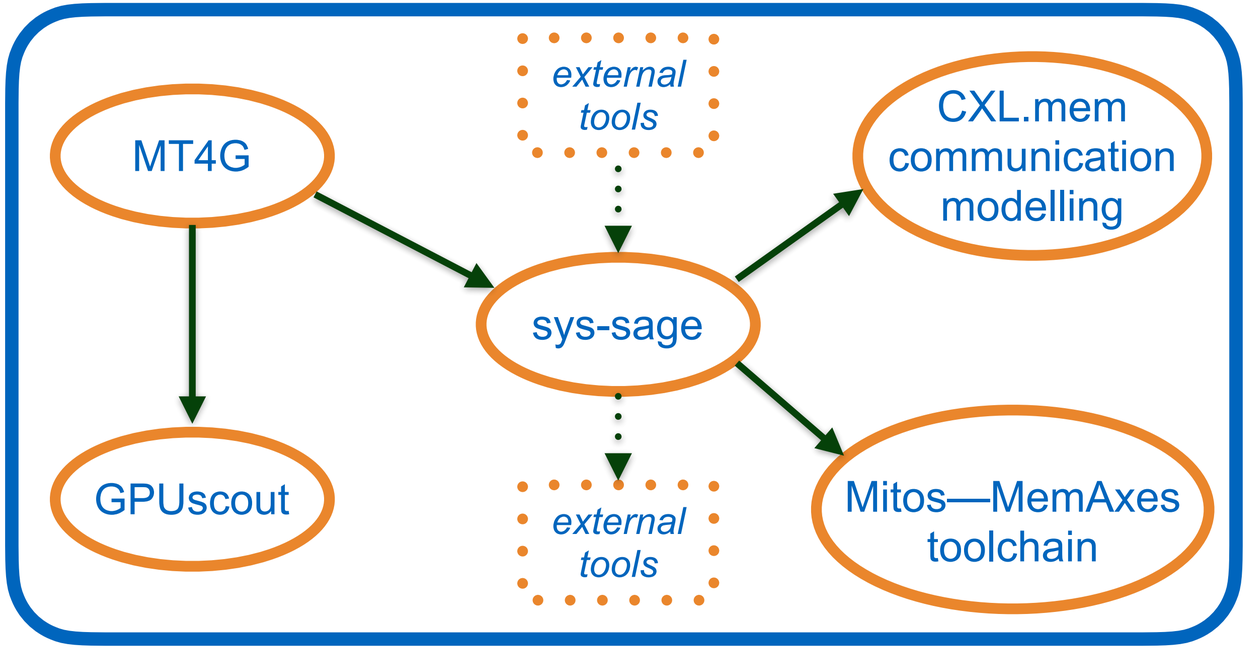
4 Main Efforts/Tools:

MT4G (GPU topology discovery)

sys-sage (system topology information management)

GPUscout (GPU memory-related bottleneck analysis)

CXL.mem communication modelling
(Modelling cross-node data transfer over CXL)



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Abstract

To solve increasingly complex problems more efficiently, modern HPC systems feature highly heterogeneous components: CPUs, GPUs, and recently QPUs (Quantum Processing Units), each with a unique, complex compute topology. The massive parallelism of GPUs, combined with emerging memory technologies on CPUs and GPUs, makes the memory topologies increasingly heterogeneous, complex, and dynamically configurable. Understanding these topological details, especially regarding available memory and its usage, is essential to operating the systems and applications efficiently.

This thesis presents a framework targeting several fundamental gaps in the currently available research and tooling: sys-sage, MT4G, GPUscout, and Mitos modeling. At the core, the sys-sage library offers a unified approach to maintaining static and dynamic topological information from different sources and APIs. Its universal architecture handles CPUs, GPUs, and QPUs alike.

MT4G provides an otherwise unavailable, vendor-agnostic, and complete report on GPU memory topologies, integrable with sys-sage. GPUs' massive parallelism amplifies the potential performance penalties of improper cache and memory usage. Therefore, GPUscout identifies root causes of frequently-occurring memory-related bottlenecks, helping users efficiently utilize the complex memory subsystem of GPUs.

Finally, to address emerging memory technologies, such as CXL.mem, this thesis presents a novel data access modeling workflow as an extension of Mitos. The model predicts the performance impact of CXL.mem-based cross-node shared-buffer data exchange as an alternative to point-to-point MPI communication.

Altogether, these tools capture topologies of HPC systems and provide missing insights into application data transfer behavior.