Computational Science and Engineering

Final Exam in Computer Architecture and Networks

Winter Term 2011/2012
February 6, 2012

Total score: 120 points

Time: 90 minutes

Instructions:

Write all answers onto these sheets – no other answers will be counted! You will get additional scratch paper to work out your solutions, however, this will not be collected and not be counted!

This exam is a **closed book** exam- i.e. no books, notes, or similar aids and also no electronic calculators of any kind are permitted!

Please do not use red or green pens.

In case you need to leave the room, you need to deposit your test sheet. Only one person is allowed to leave the room at one time.

There will be an announcement 10 minutes before the end of the test time.

After the test, please remain seated until all tests have been collected and counted.

Name: _____

Matr. Number: _____

Signature: _____

Question 1, Numbering Systems (10 points):

In the following table, each row represents the same (positive) number represented in a different numbering system. The numbering system is denoted in the upper row. Complete the table by filling in the missing number representations!

Binary	Octal	Decimal	Hexadecimal
11001101			
	777		
		20	
			BAAB

Question 2, PC Hardware (30 points):

Outline the basic structure of a superscalar microprocessor with typical units:

Illustration

Give two examples of state of the art x86 superscalar processors ! What are their main conceptual differences ?

Question 3, Execution Models:

Explain the stack principle and give some examples where it is being used!

What is its major drawback?

How is

C = A + B

translated into machine code on an ARM architecture? Which execution model is this?

How is

C = A + B

translated into machine code on a VAX architecture? Which execution model is this?

Question 4, Pipelining (12 points):

Explain the difference between a standard pipeline, a superscalar pipeline and a VLIW pipeline by drawing an illustration for each case:

a) Standard Pipeline:

b) Superscalar Pipeline

c) VLIW Pipeline

Question 5, Cache (30 points):

Why are modern processors using caches? What are their advantages and disadvantages?

What is an n-way set associative mapping?

Given a cache line number of m, what are a 1-way set associative cache and an m-way set associative cahes?

What are *rotating registers* used for? Explain how an Itanium processor uses them!

Explain the difference between *data speculation* and *control speculation*! Where is an *Advanced Load Address Table* being used?

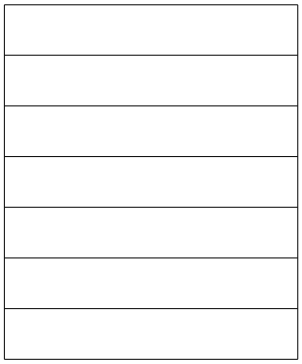
Question 5, Processor/Architecture Development (15 points):

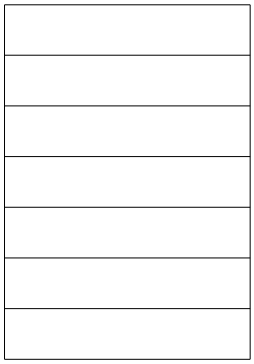
Moore's law states that the number of transistors on a chip doubles every 1 ½ years. While this led to an increase of clock frequencies without much need to rewrite you programs in order to obtain better performance, why was this trend stoppd a few years ago? What did vendors do with the increasing number of transistors?

What do the terms *Little Endian* and *Big Endian* stand for? Which approach is better?

Question 6, Networks (15 points):

Outline the ISO/OSI seven layer model being used as a generic model for computer networks:





Are all 7 layers used in the TCP/IP protocol suite?