Dr. Eishi **Arima**

Scientific Staff (Wissenschaftliche Mitarbeiter)

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Work Experience

Employment

Technical University of Munich (Technische Universität München) — *Garching, Germany*

Scientific Staff (Wissenschaftliche Mitarbeiter) — *Apr. 2021 - present*

- Informatics 10, Department of Informatics

The University of Tokyo — *Tokyo, Japan*

Project Research Associate (or Project Assistant Professor) — *Apr. 2016 - Mar. 2021*

- Supercomputing Research Division, Information Technology Center

The University of Tokyo — *Tokyo, Japan*

Research Assistant — *Apr. 2012 - Mar. 2016*

- Graduate School of Information Science and Technology

Guest Scientist

Technical University of Munich (Technische Universität München) — *Garching, Germany*

External Scientist — *Jun. 2018 - Mar. 2019*

- Informatics 10, Department of Informatics

Lawrence Livermore National Laboratory — *CA, US*

Visiting Scientist — *Oct. 2016 - Oct. 2017*

- Center for Applied Scientific Computing

RIKEN R-CCS — *Hyogo, Japan*

Visiting Scientist — *May. 2016 - Mar. 2021*

- Architecture Development Team

Education

The University of Tokyo — *Tokyo, Japan*

Ph.D in Information Science and Technology — *Mar. 2016*

- Cache Design Optimization for Energy-Efficient Processors

The University of Tokyo — *Tokyo, Japan*

Master of Information Science and Technology — *Mar. 2013*

- Power Reduction of Cache Memory in Idle State

The University of Tokyo — *Tokyo, Japan*

Bachelor of Engineering — *Mar. 2011*

- A High-Resolution Book Digitization System Based on High-Speed 3D Shape Recognition

Research Summary

My broader research interests are principally in computer architecture, system software, and high performance computing (HPC), while the recent major focuses are on (1) resource/power management in HPC systems; (2) heterogeneous system/processor/memory architectures; (3) performance/power modeling, analysis, and optimization; and (4) software/hardware interactions and interfaces. In particular, I am currently involved in REGALE project and am responsible for designing the entire software architecture in order to realize a holistic and sophisticated resource management for large-scale HPC systems. In addition to the above areas, I have conducted a variety of microarchitecture-level hardware studies including (1) memory

system design optimizations based on emerging device technologies and (2) evaluations and design space explorations for SIMD-based HPC microprocessors.

Grants & Awards

FY2020-FY2021	**PI**, "Coscheduling Methods for Next-Generation Large-Scaled Systems with Heterogeneous Memories", JSPS Grant-in-Aid for Early-Career Scientist, No.20K19766, 4.29M JPY (**acceptance rate: 7496/18708=40.1%**)	*JSPS, Japan*
FY2018-FY2020	**PI**, "Exploiting High-Bandwidth and Large-Capacity on Hybrid Main Memories through Pattern-Aware Optimization", JSPS Grant-in-Aid for Early-Career Scientist, No.18K18021, 4.16M JPY (**acceptance rate: 6256/20369=30.7%**)	*JSPS, Japan*
FY2016-FY2017	**PI**, "Memory System Optimzation for Energy Efficient Big Data Processing", JSPS Grant-in-Aid for Research Activity Start-up, No.16H06677, 2.99M JPY (**acceptance rate: 925/3699=25.0%**)	*JSPS, Japan*

Professional Activities

Organizing Committee: ACM CF 2023 (Publicity Co-Chair); HPC ASIA 2022 (Architecture Track Co-Chair); ACM CF 2021 (Special Session Co-Chair); ACM CF 2020 (Program Co-Chair); IEEE CLUSTER 2019 (Publications Chair); IEEE NVMSA 2018 (Web Chair)

Program Committee: IEEE HiPC 2022; CANDAR 2022; xSIG 2022 (JP domestic); IEEE NVMSA 2022; ACM CF 2022; IEEE IPDPS 2022; CANDAR 2021; IEEE NVMSA 2021; ISC 2021 PhD Forum; xSIG 2021 (JP domestic); IEEE IPDPS 2021 (system software track); IEEE IPDPS 2021 (programming model track); HPCAsia 2021; IEEE HiPC 2020; IA^3@SC 2020; CANDAR 2020; IEEE Cluster 2020 (posters); ISC 2020 PhD Forum; xSIG 2020 (JP domestic); CANDAR 2019; ISC 2019 PhD Forum; xSIG 2019 (JP domestic); CANDAR 2018; ICPP 2018; IEEE NVMSA 2018; SCAsia 2018; HPCAsia 2018; CANDAR 2017; IEEE NVMSA 2017

Steering Committee: HPC PowerStack (2021-); IEICE CPSY (Assistant Secretary, 2019-2021); IPSJ SIGARC (2016-2020)

Journal Reviews: Journal of Parallel and Distributed Computing (2021); Concurrency and Computation: Practice and Experience, Wiley (2021); The Journal of Supercomputing, Springer (2020-); Elsevier Integration, the VLSI Journal (2019); IPSJ Transactions on Advanced Computer Systems (2017-); IEICE Transactions on Information and Systems (2016-)

Student Mentoring

2022	**Master's Thesis**, Faith, Rifqi Al "Optimizing Memory Capacity/Bandwidth Priorities on Modern CPU via Machine Learning"	*TUM, Germany*
2022	**Master's Thesis**, Stobbe, Adrian "Dealing with Resource Limits for a HPC Jobs in a Distributed System"	*TUM, Germany*
2022	**Master's Thesis**, Saba, Issa "Job Co-location and Power Budgeting for Heterogeneous HPC Systems"	*TUM, Germany*
2022	**Master's Thesis**, Terkin, Tuana "Memory-footprint aware co-scheduling for HPC clusters"	*TUM, Germany*
2022	**Guided Research**, Krisko, Milan "Probabilistic Hardware Performance Counters"	*TUM, Germany*
2022	**Bachelor's Thesis**, Kang, Minjoon "Co-scheduling for Modern GPUs under Power Caps"	*TUM, Germany*
2022	**Bachelor's Thesis**, Balakirev, Aleksandr "Exploring the Benefits of Non-volatile Memory in HPC Applications" (Led by Dr. Josef Weidendorfer)	*TUM, Germany*

Publications and Talks

Publications

1. Issa Saba, Eishi Arima, Dai Liu, Martin Schulz "Orchestrated Co-Scheduling, Resource Partitioning, and Power Capping on CPU-GPU Heterogeneous Systems via Machine Learning", In *Proceedings of 35th GI/ITG International Conference on Architecture of Computing Systems (ARCS)*, pp.xxx-xxx, Sep., 2022 (to appear)
2. Eishi Arima, Minjoon Kang, Issa Saba, Josef Weidendorfer, Carsten Trinitis, Martin Schulz "Optimizing Hardware Resource Partitioning and Job Allocations on Modern GPUs under Power Caps", In *Proceedings of International Conference on Parallel Processing Workshops*, pp.xxx-xxx, Aug., 2022 (to appear)
3. Eishi Arima, Isaías A Comprés, Martin Schulz "On the Convergence of Malleability and the HPC PowerStack: Exploiting Dynamism in Over-Provisioned and Power-Constrained HPC Systems", In *Proceedings of ISC High Performance Workshops*, pp.xxx-xxx, Jun., 2022 (to appear)
4. Eishi Arima, Carsten Trinitis, Martin Schulz "Toward Dynamic Orchestration of Data/Power/Process Management for Hybrid Memory Based Systems", In *Tagungsband des FG-BS Herbsttreffens*, 3pages, Sep., 2021

5. Eishi Arima, Yuetsu Kodama, Tetsuya Odajima, Miwako Tsuji, Mitsuhisa Sato, "Power/Performance/Area Evaluations for Next-Generation HPC Processors using the A64FX Chip", In *Proceedings of IEEE Symposium on Low-Power and High-Speed Chips and Systems*, 6pages, Apr., 2021
6. Yuetsu Kodama, Tetsuya Odajima, Eishi Arima, Mitsuhisa Sato, "Evaluation of Power Management Control on the Supercomputer Fugaku", In *Proceedings of 2020 IEEE International Conference on Cluster Computing (CLUSTER)*, EEHPC volume, pp. 484-493, Sep., 2020
7. Eishi Arima, "Classification-Based Unified Cache Replacement via Partitioned Victim Address History", In *Proceedings of 2020 23rd Euromicro Conference on Digital System Design (DSD)*, pp.101-108, Aug., 2020
8. Eishi Arima, Toshihiro Hanawa, Carsten Trinitis, Martin Schulz, "Footprint-Aware Power Capping for Hybrid Memory Based Systems", In *Proceedings of the 35th International Conference on High Performance Computing, ISC High Performance 2020 (**ISC**)*, pp.347-369, Jun., 2020 (**acceptance rate: 27/87=31%**)
9. Eishi Arima, Martin Schulz, "Pattern-Aware Staging for Hybrid Memory Systems", In *Proceedings of the 35th International Conference on High Performance Computing, ISC High Performance 2020 (**ISC**)*, pp.474-495, Jun., 2020 (**acceptance rate: 27/87=31%**)
10. Hiroki Noguchi, Kazutaka Ikegami, Satoshi Takaya, Eishi Arima, Atsushi Kawasumi, Hiroyuki Hara, Keiko Abe, Naoharu Shimomura, Junichi Ito, Shinobu Fujita, Takashi Nakada, Hiroshi Nakamura, "4Mb STT-MRAM-based Cache with Memory-Access-aware Power Optimization and Novel Write-Verified-Write / Read-Modified-Write Scheme", In *Proceedings of 2016 IEEE International Solid-State Circuits Conference (**ISSCC**)*, pp.132–133, Feb., 2016 (**acceptance rate: 200/595=34%**)
11. Susumu Takeda, Hiroki Noguchi, Kumiko Nomura, Shinobu Fujita, Shinobu Miwa, Eishi Arima, Takashi Nakada, Hiroshi Nakamura, "Low-power cache memory with state-of-the-art STT-MRAM for high-performance processors", In *Proceedings of the 12th International SoC Design Conference (ISOCC)*, pp.153–154, Nov., 2015
12. Eishi Arima, Hiroki Noguchi, Takashi Nakada, Shinobu Miwa, Susumu Takeda, Shinobu Fujita, Hiroshi Nakamura, "Immediate Sleep: Reducing Energy Impact of Peripheral Circuits in STT-MRAM Caches", In *Proceedings of the 33rd IEEE International Conference on Computer Design (**ICCD**)*, pp.149–156, Oct. 2015 (**acceptance rate: 83/269=31%**)
13. Hiroki Noguchi, Kumiko Nomura, Keiko Abe, Shinobu Fujita, Eishi Arima, Kyundong Kim, Takashi Nakada, Shinobu Miwa, Hiroshi Nakamura, "D-MRAM Cache: Enhancing Energy Efficiency with 3T-1MTJ DRAM/MRAM Hybrid Memory", In *Proceedings of Design, Automation & Test in Europe Conference & Exhibition (**DATE**)*, pp.1813–1818, Mar., 2013 (**acceptance rate: 206/829=25%**)
14. Eishi Arima, Toshiya Komoda, Takashi Nakada, Shinobu Miwa, Hiroki Noguchi, Kumiko Nomura, Keiko Abe, Shinobu Fujita, Hiroshi Nakamura, "Analyzing Requirements Specification of STT-MRAM Last Level Cache Considering Low CPU Loads", *IEICE Transactions*, Vol.J97-A, No.10, pp.629-647, 2014 (in Japanese)
15. Eishi Arima, Toshiya Komda, Takashi Nakada, Shinobu Miwa, Hiroshi Nakamura, "Lost Data Prefetching to Reduce Performance Degradation Caused by Powering off Caches", *IPSJ Transaction of Advanced Computing Systems*, Vol.6, No.3, pp.118-130, 2013 (in Japanese)

Conference Posters or Workshop Presentations (Refereed)

16. Eishi Arima, Carsten Trinitis, "A Case for Co-Scheduling for Hybrid Memory Based Systems", *48th International Conference on Parallel Processing (ICPP)*, Poster Session, Aug., 2019
17. Eishi Arima, Toshihiro Hanawa, Martin Schulz, "Toward Footprint-Aware Power Shifting for Hybrid Memory Based Systems", *47th International Conference on Parallel Processing (ICPP)*, Poster Session, Aug., 2018
18. Eishi Arima, Hiroshi Nakamura, "Page Table Walk Aware Cache Management for Efficient Big Data Processing", *Big Data Benchmarks, Performance Optimization, and Emerging Hardware (BPOE-8) (in conjunction with 22nd ACM International Conference on Architectural Support for Programming Languages and Operating Systems)*, Apr., 2017
19. Eishi Arima, Hiroki Noguchi, Takashi Nakada, Shinobu Miwa, Susumu Takeda, Shinobu Fujita, Hiroshi Nakamura, "Subarray Level Power-Gating in STT-MRAM Caches to Mitigate Energy Impact of Peripheral Circuits", *52nd ACM/EDAC/IEEE Design Automation Conference (DAC)*, Work-in-Progress Session, June, 2015
20. Eishi Arima, Hiroki Noguchi, Takashi Nakada, Shinobu Miwa, Susumu Takeda, Shinobu Fujita, Hiroshi Nakamura, "Fine-Grain Power-Gating on STT-MRAM Peripheral Circuits with Locality-aware Access Control", *The Memory Forum (in conjunction with the 41st International Symposium on Computer Architecture)*, June, 2014

Invited Talks

21. Speaker at "BoF: Community-Driven Efforts for Energy Efficiency in HPC Software Stack", SC'22, Nov., 2022
22. Eishi Arima, "REGALE: An open architecture to equip next generation HPC applications with exascale capabilities –Technical Overview", HPC PowerStack Seminar, Nov., 2022
23. Eishi Arima, "REGALE: Holistic and Feedback-driven Resource Management for Efficient Application Execution at Exascale", HeLP-DC at HiPEAC'22, Jun., 2022
24. Eishi Arima, "REGALE: An open architecture to equip next generation HPC applications with exascale capabilities", E4 booth at ISC'22, Jun., 2022
25. Panelist at "BoF: Community-Driven Efforts for Energy Efficiency in HPC Software Stack", SC'21, Nov., 2021

26. Eishi Arima, “Ongoing Efforts on Co-scheduling and Holistic Power Management”, Adaptive Resource Management for HPC Systems (Dagstuhl Seminar 21441), Nov., 2021
27. Eishi Arima, “HW/SW Optimizations for Emerging Systems: Memory Perspective”, LBNL - U. Tokyo Meeting, Sep. 2019
28. Eishi Arima, “Optimizations for Computing Systems with Emerging Memory Technologies”, The Asia Pacific Society for Computing and Information Technology (APSCIT), Jul. 2019
29. Eishi Arima, “Efficient Big Data Processing through Page Table Walk Aware Cache Management”, ASE Seminar, Apr. 2017
30. Eishi Arima, “Revisiting Memory Systems for Energy-Efficient Supercomputers”, LLNL CASC Seminar, Oct. 2016